Current Sensorless Control Algorithm for Single-Phase Three-Level NPC Inverter

Alexander Suzdalenko (*Researcher, Riga Technical University*), Janis Zakis (*Leading researcher, Riga Technical University*), Ingars Steiks (*Leading researcher, Riga Technical University*)

***Abstract* – Current measurement becomes challenging task in power converters operating at high switching frequencies, moreover traditional control system requires two control loops – first (slow) regulates DC-link voltage, second (fast) controls the shape of current, that all together results in complicated transfer function and long transition periods. The current sensorless control (CSC) allows neglecting mentioned problems. This research delivers solution of CSC implementation in single-phase three-level neutral point clamped inverter for the first time. Mathematical equations have been defined for inductor current peaks and transistor conduction time during discontinuous and continuous conduction modes, as well as, major problem of current fitting between different voltage levels (consequently with different current peak-to-peak values) was solved, providing two solutions – pre-fitting and post-fitting trajectories. The verification of our theoretical assumptions and analytical equations were confirmed by the simulation analysis. Challenges of real experiments are discussed in the conclusions.**

***Keywords* – sensorless control, current control, pulse width modulation inverters.**

I. Introduction

New technologies of power electronic switches allows designing switched mode power supplies (SMPS) operating at higher switching frequencies that leads to minimization of reactive components and increase of power density of power converters. However, current measurement becomes new challenge when operates at frequencies above 100 kHz. For instance, galvanically isolated current sensors inherit signal's propagation delay, as well as, limited bandwidth. The use of shunt resistor eliminates mentioned problems, but on the other hand, leads to additional conduction loses that negatively influence the efficiency of the converter. Thus, elimination of instantaneous current measurement would allow overcoming mentioned problems, as well as, reducing the cost and size of the control system accordingly to [1]–[4].

Moreover, traditional control system usually consist of two control loops – the first one (slow) controls the capacitor voltages on the DC link, while second one (fast) controls the shape of current. This results in complicated transfer function, as well as, long transient responses, while current sensorless control (CSC) excludes current control loop, that leads to simpler control system of the converter [5], [6].

The CSC method was mostly applied to power factor correction circuit based diode rectifier and boost converter [5]–[7]. Recent publication demonstrated good performance of CSC applied to bidirectional AC/DC converter based on full-bridge converter [8]. All of mentioned papers limited their investigation with only inductor's continuous conduction mode (CCM) selecting either bulky inductor, either selecting higher switching frequency. Author's previous publications [9], [10] has described the CSC use with half-bridge converter, where among other attention is also focused on current control during DCM. Contrary to previous topologies, the inductor in half-bridge converter experiences higher voltage, as a result, current slopes has more impetuous rising and falling edges that leads to longer DCM period, that should not be neglected. The comparison of mentioned papers is made in the Table I.

A lot of decades three-level neutral point clamped (NPC) topology has been used in electrical drive applications [11]–[13], but since the increase of renewable energy applications, NPC has also found it use here [14], [15]. Application of CSC with NPC converters seems relevant, as on the one hand, inductor is exposed to smaller voltage stresses that provides earlier CCM than, for instance, in full-bridge topology and, as a result, simple CSC calculations. On the other hand, due to switching between different voltage levels, the inductor's current peak-to-peak value changes, that should be specially treated, ensuring that average inductor's current value will track the reference signal. Overviewing different control techniques of NPC converters [16]–[21], none of them delivers CSC. Interesting that in [22] sensorless current control is discussed, however, the sinusoidal carrier-based PWM is utilized and multiple simplifications are assumed, giving no sense on real CSC.

This paper is organized as follows: the second section introduces the main theory of CSC. Third section demonstrates the simulation results. The last section discusses the results and points out challenges for real experiments.

TABLE I
COMPARISON OF DIFFERENT CSC PROJECTS

		[5]	[7]	[6]	[8]	[9]
Topology		Boost	Boost	Boost	Full-bridge	Half-bridge
Immunity from non-sinusoidal voltage		-	-	√	√	√
Current control	DCM	-	-	-	-	√
	CCM	√	√	√	√	√
Switching frequency [kHz]		25	160	50	40	25
Inductance [mH]		4.65	1.2	4.56	4.6	2
Capacitance [mF]		0.56	2.2	0.47	1.4	(2x) 1
Power (W)		500	400	500	500	1000
AC voltage (RMS)		110	55	110	110	220
DC voltage		300	100	300	200	750

II. Theory of CSC applied for MLC

The main idea of CSC is to hold proper Volts-second balance on inductor, in order to keep average current value to track reference signal. Contrary to full-bridge or half-bridge converters, where either full DC-link voltage either freewheeling state is applied to inductor, the MLC has its superior feature of selecting the voltage level (1 V_{DC}, ½ V_{DC}, 1/3 V_{DC}, ¼ V_{DC} depending on the number of levels) that is applied to inductor. In this research single-phase three-level neutral-point-clamped (NPC) inverter is studied. Taking into account, that current can be boosted to the grid, when voltage applied to inductor is higher than grid's voltage, three combination of commutated switches has been defined seen in Table II. It demonstrates commutated current paths and corresponding voltage applied to inductor in respect to different input voltage ranges during positive half-period of input voltage. The Table III summarizes all switching combinations during whole period of input voltage.

TABLE II

COMMUTATED CURRENT PATHS AND CORRESPONDING INDUCTOR VOLTAGE DURING POSITIVE INPUT VOLTAGE HALF-PERIOD

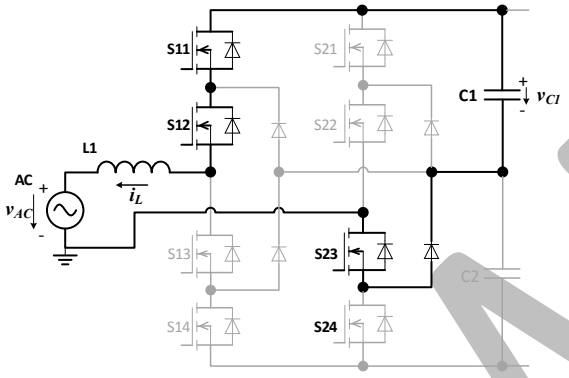
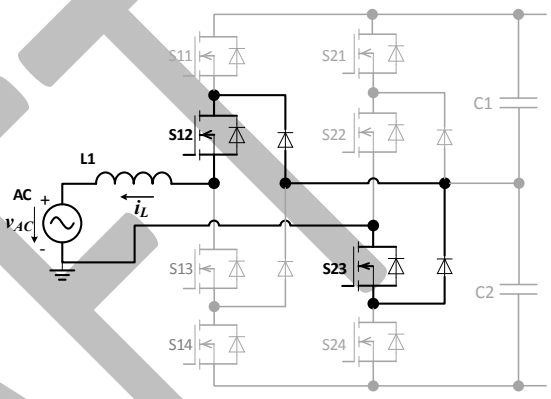
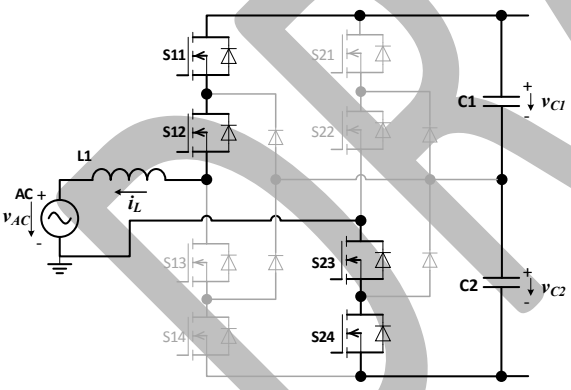
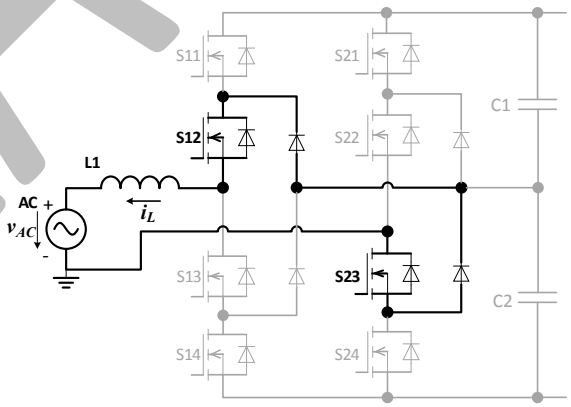
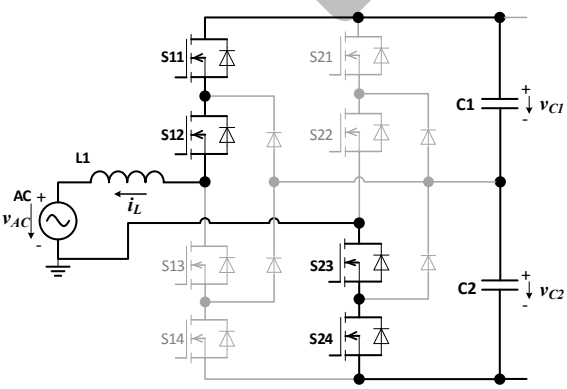
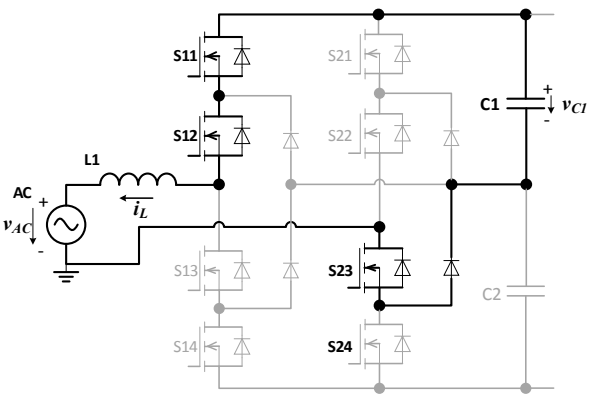
	Boosting energy (*d=1*)	Freewheeling (*d=0*)
$V_{AC}<0.8*V_{C1}$		
	$V_L=V_{C1}-V_{AC}$	$V_L=-V_{AC}$
$0.8*V_{C1}<V_{AC}<1.2*V_{C1}$		
	$V_L=V_{C1}+V_{C2}-V_{AC}$	$V_L=-V_{AC}$
$V_{AC}>1.2*V_{C1}$		
	$V_L=V_{C1}+V_{C2}-V_{AC}$	$V_L=V_{C1}-V_{AC}$

TABLE III
SUMMARY OF SWITCHING SIGNAL COMBINATION AND CORRESPONDING INDUCTOR VOLTAGE

Input voltage polarity	Input voltage level	Current path $d(t)$	S11	S12	S13	S14	S21	S22	S23	S24	Inductor's voltage
Positive	$V_{AC}<0.8*V_{C1}$	1	1	1	-	-	-	-	1	-	$V_L=V_{C1}-V_{AC}$
		0	-	1	-	-	-	-	1	-	$V_L=-V_{AC}$
	$0.8*V_{C1}<V_{AC}<1.2*V_{C1}$	1	1	1	-	-	-	-	1	1	$V_L=V_{C1}+V_{C2}-V_{AC}$
		0	-	1	-	-	-	-	1	-	$V_L=-V_{AC}$
	$V_{AC}>1.2*V_{C1}$	1	1	1	-	-	-	-	1	1	$V_L=V_{C1}+V_{C2}-V_{AC}$
		0	1	1	-	-	-	-	1	-	$V_L=V_{C1}-V_{AC}$
Negative	$-V_{AC}<0.8*V_{C2}$	1	-	-	1	1	-	1	-	-	$V_L=V_{C2}+V_{AC}$
		0	-	-	1	-	-	1	-	-	$V_L=V_{AC}$
	$0.8*V_{C2}<-V_{AC}<1.2*V_{C2}$	1	-	-	1	1	1	1	-	-	$V_L=V_{C1}+V_{C2}+V_{AC}$
		0	-	-	1	-	-	1	-	-	$V_L=V_{AC}$
	$-V_{AC}>1.2*V_{C2}$	1	-	-	1	1	1	1	-	-	$V_L=V_{C1}+V_{C2}+V_{AC}$
		0	-	-	1	1	-	1	-	-	$V_L=V_{C2}+V_{AC}$

In order to track the changes of polarity of different variables in digital control system, simple Boolean function is defined as follows

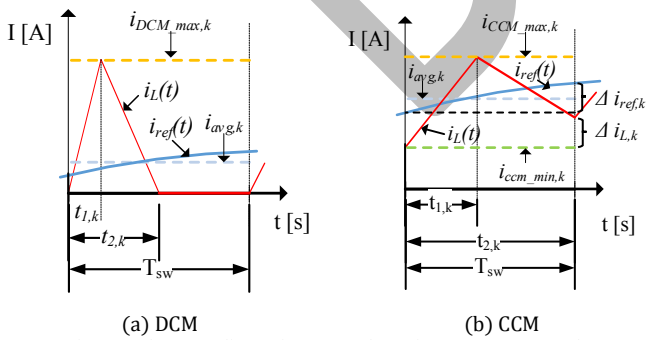
$$pos(x)=\begin{cases}0, if\ x<0\\ 1, if\ x\geq 0\end{cases}. \quad (1)$$

Now it is possible to write versatile inductor's voltage equations that combine all variation from Table III as follows

$$\begin{aligned}v_L(d=1)=&-(2\cdot pos(V_{AC})-1)\cdot V_{AC}+\\&+pos(V_{AC})\cdot pos(-V_{AC}+0.8\cdot V_{C2})\cdot V_{C1}+\\&+pos(-V_{AC})\cdot pos(V_{AC}+0.8\cdot V_{C1})\cdot V_{C2}+\\&+(pos(V_{AC}-0.8\cdot V_{C1})\,or\ pos(-V_{AC}-0.8\cdot V_{C2}))\cdot(V_{C1}+V_{C2})\end{aligned}, \quad (2)$$

$$\begin{aligned}v_L(d=0)=&-(2\cdot pos(V_{AC})-1)\cdot V_{AC}\\&+pos(V_{AC}-1.2\cdot V_{C1})\cdot V_{C1}+pos(-V_{AC}-1.2\cdot V_{C2})\cdot V_{C2}\end{aligned}. \quad (3)$$

The Fig. 1 demonstrates discontinuous and continuous current modes for input inductor that also has certain influence on average current calculation equations.



(a) DCM (b) CCM

Fig. 1. Inductor's discontinuous and continuous current modes.

The peak value of inductors current can be described by two formulae as follows

$$i_{DCM\_max,k}=\frac{V_{L,k}(d=1)}{L}\cdot t_{1,k}, \quad (4)$$

$$-i_{DCM\_max,k}=\frac{V_{L,k}(d=0)}{L}\cdot(t_{2,k}-t_{1,k}), \quad (5)$$

where from $t_{2,k}$ is defined as

$$t_{2,k}=\frac{V_{L,k}(d=0)-V_{L,k}(d=1)}{V_{L,k}(d=0)}. \quad (6)$$

The average current can be calculated as simple area of triangle divided by period as follows

$$i_{ref,k}=i_{avg,k}=\frac{i_{DCM\_max,k}\cdot t_{2,k}}{2\cdot T_{sw}}. \quad (7)$$

Substituting the $t_{2,k}$ in (7) by the definition in (6) and extracting transistor's conduction time, the following control law is defined

$$t_{1,k}=\sqrt{\frac{i_{avg,k}\cdot L\cdot 2\cdot T_{sw}\cdot V_{L,k}(d=0)}{V_{L,k}(d=1)\cdot(V_{L,k}(d=0)-V_{L,k}(d=1))}}. \quad (8)$$

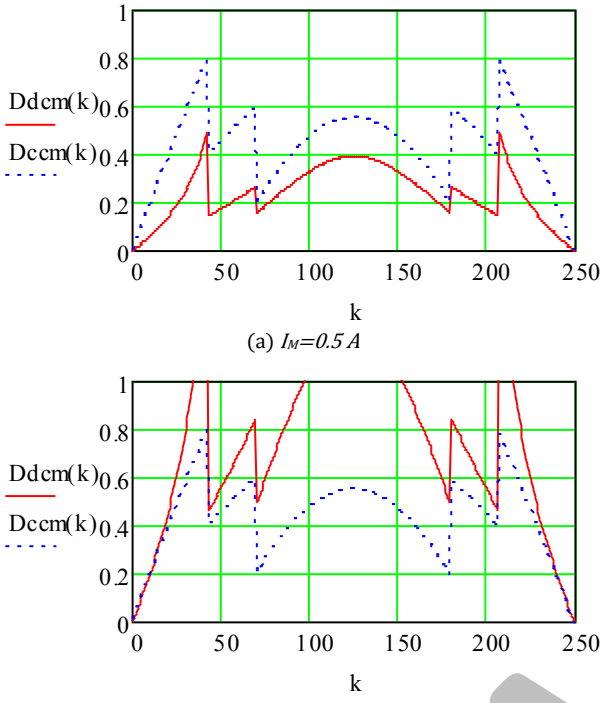
The CCM control law can be extracted from the equation of volt-second balance during single switching period, which is defined as

$$\Delta i_{ref,k}=\frac{V_{L,k}(d=1)}{L}\cdot t_{1,k}+\frac{V_{L,k}(d=0)}{L}\cdot(T_{sw}-t_{1,k}). \quad (9)$$

So, the transistor's conduction time in CCM is defined as

$$t_{1,k}=\frac{\Delta i_{ref,k}\cdot L-V_{L,k}(d=0)\cdot T_{sw}}{V_{L,k}(d=1)-V_{L,k}(d=0)}. \quad (10)$$

The Fig. 2 demonstrates analytical waveforms of DCM and CCM control laws for rectifier and inverter mode. The final commutation signal is selected as minimal value of DCM and CCM signals.



(a) $I_M=0.5\ A$

(b) $I_M=5\ A$

Fig. 2. Analytical waveforms of duty cycle for half-period of input voltage (index k represents switching cycle serial number, $f_{AC}=50\ Hz$, $f_{SW}25\ kHz$, $V_{AC\_M}=311\ V$, $V_{C1}(t=0)=V_{C2}(t=0)=200\ V$, $L=1\ mH$)

Additional attention should be focused on transition between the different voltage levels during CCM, as peak-to-peak current value is also changing. It means that special volt-second balance should be applied during transition between different voltage level switching, in order to keep inductor's average current value to track reference signal. The Fig. 3. demonstrates two possible trajectories for current fitting at transition between different voltage levels.

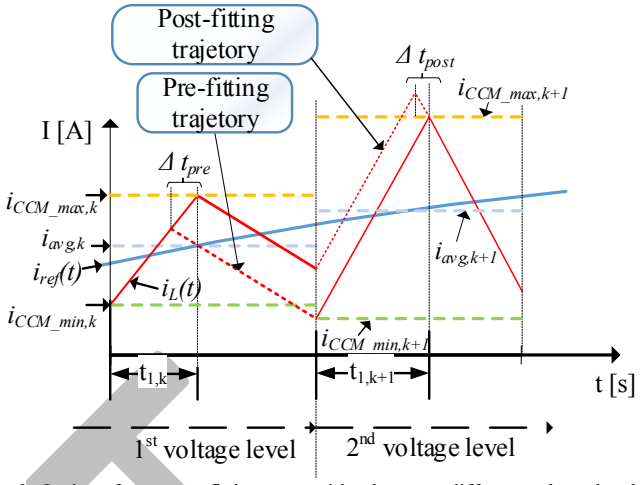


Fig. 3. Options for current fitting at transition between different voltage levels.

Both pre- and post-fitting duty-cycle corrections are calculated by (10), where besides $\Delta i_{ref,k}$ the differences between current peak-to-peak values (of falling edges) at different voltage levels should be taken into account as follows (equation for post-fitting)

$$t_{1,k+1}=\frac{\left(\Delta i_{ref,k+1}-\frac{i_{fal,k}-i_{fal,k+1}}{2}\right)\cdot L-V_{L,k+1}(d=0)\cdot T_{sw}}{V_{L,k+1}(d=1)-V_{L,k+1}(d=0)}, \quad (11)$$

where $i_{fal,k}$ is calculated similarly as in (5), substituting $t_{2,k}$ with commutation period T_{SW} as follows

$$i_{fal,k}=\frac{V_{L,k}(d=0)\cdot(T_{SW}-t_{1,k})}{L}. \quad (12)$$

III. Simulation Results

The PSIM simulation software was used to study the proposed CSC algorithm, which was coded in "Simplified C Block". The open loop control was assembled fast evaluation, as well as voltage sources was used instead of capacitors. The overall schematic is seen in the Fig. 4.

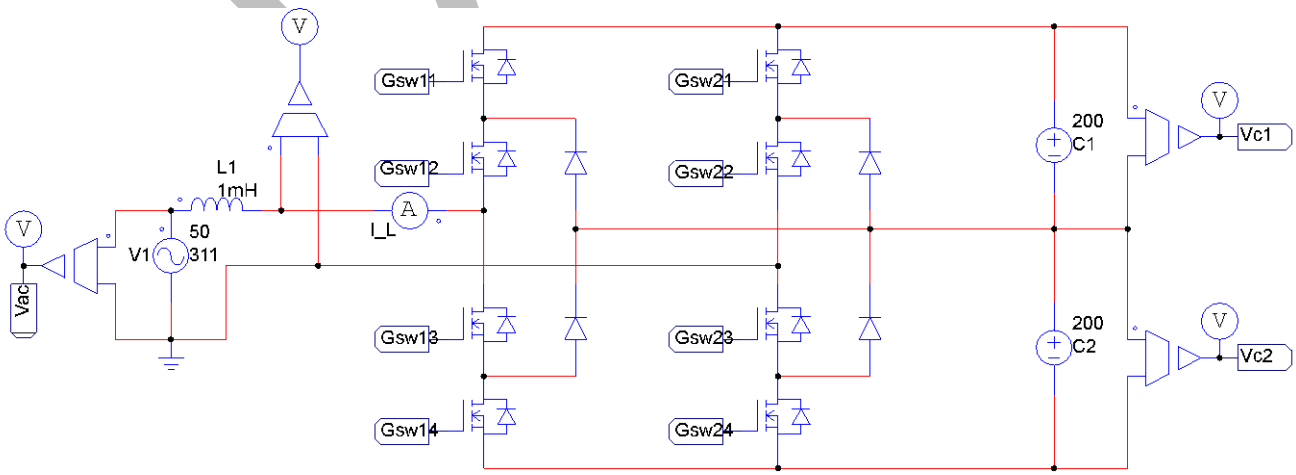
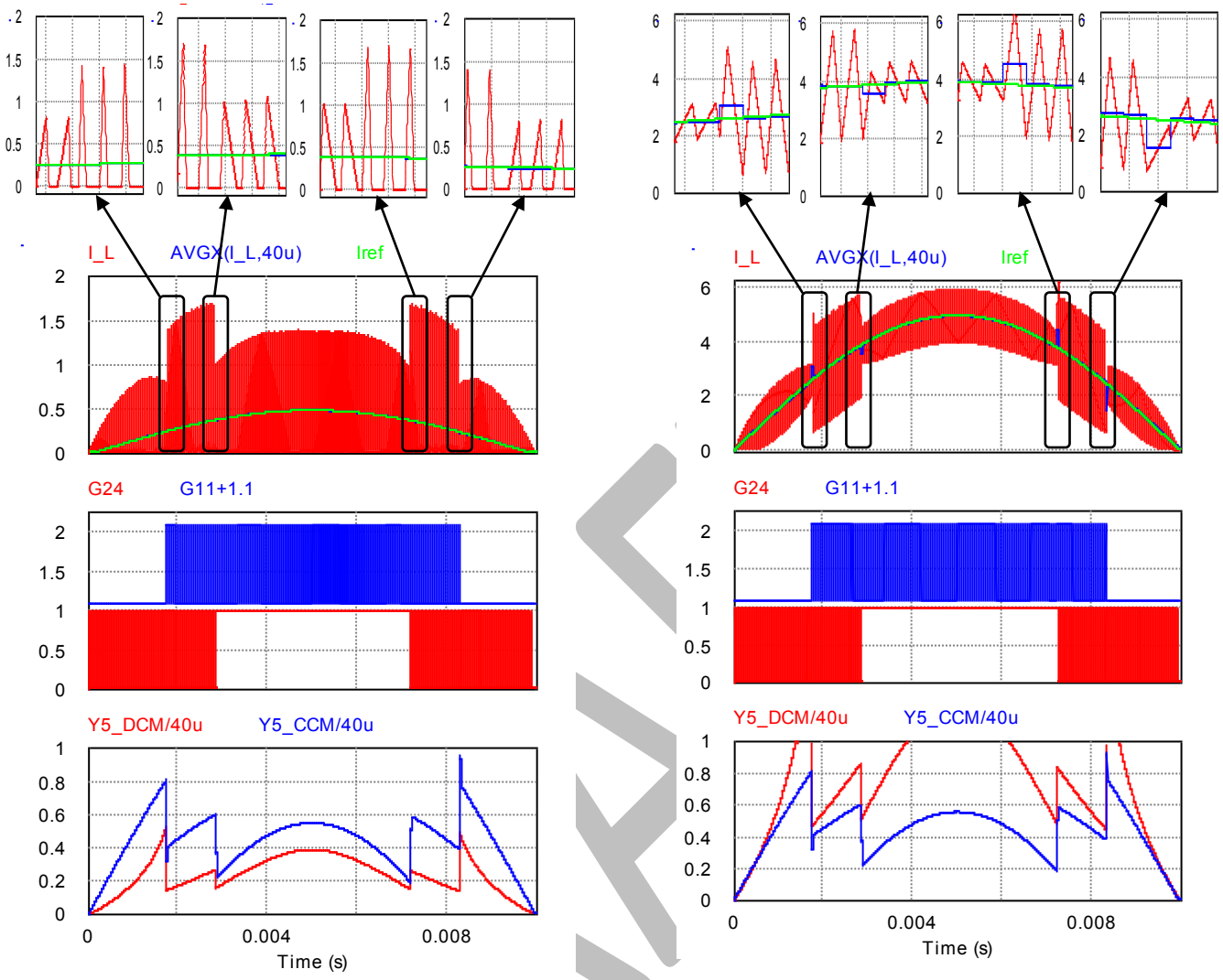


Fig. 4. Power part of the simulation model (ideal elements are utilized).



(a) Reference current amplitude I_M=0.5 A

(b) Reference current amplitude I_M=5 A

Fig. 5. Simulation results of CSC applied to NPC inverter during (a) DCM and (b) CCM operation (top graphs (I_L, AVGX(I_L,40u), Iref) consist of inductor's current, average inductor current, reference current values; middle graphs (G24, G11+1.1) contain actively commutated switching signals; bottom graphs represent)calculated DCM and CCM duty cycle values.

The Fig. 5. demonstrates the simulation results of NPC inverter operation under CSC algorithm, where duty cycle is calculated by using (8) and (10) and no current control loop is utilized in the control system. As it can be seen from Fig. 5(a) top graph the average value of inductor's current (blue) perfectly matches the reference signal (green). The same can be concluded from Fig. 5(b) top graph, where average inductor's current (blue) matches the reference signal (green), except the switching periods, when transition between different voltage levels occurs. The post-fitting current trajectory has been applied that have provided satisfied results.

IV. Conclusions

The CSC allows eliminating instantaneous current measurements in SMPS that can be useful for converters operating at high switching frequency, either to minimize the cost and size of control system.

Previously this technique was used only with two level SMPS (diode bridge with boost DC/DC converter, half-bridge, full-bridge), while hereby the theoretical model of CSC has been developed for three-level NPC multilevel inverter, where special attention was focused on proper volt-second balance during transition between different voltage levels. Two options were defined in this context – pre-fitting and post-fitting current trajectories.

The simulation results confirmed the theoretical model, consequently, ability of shaping current by using CSC was successfully simulated for DCM and CCM, as well as post-fitting current matching technique was successfully applied during transition between different voltage levels of single-phase three-level NPC converter.

The real experiment would require improvement of CSC by including conduction loses of real switching and reactive elements. Additionally, post- or pre-fitting techniques should be dynamically selected in order to have fluent change of duty cycle value.

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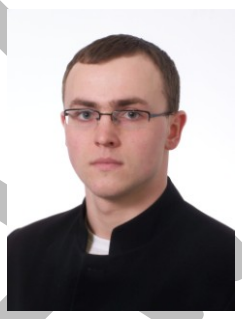

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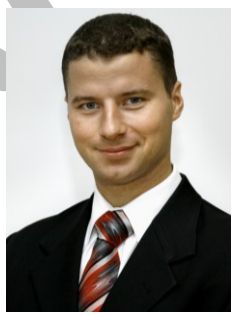

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