

Comparative Analysis of Semiconductor Power Losses of Galvanically Isolated Quasi-Z-Source and Full-Bridge Boost DC-DC Converters

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Abstract – This paper compares semiconductor losses of the galvanically isolated quasi-Z-source converter and full-bridge boost DC-DC converter with active clamping circuit. Operation principle of both converters is described. Short design guidelines are provided as well. Results of steady state analysis are used to calculate semiconductor power losses for both converters. Analytical expressions are derived for all types of semiconductor power losses present in these converters. The theoretical results were verified by means of numerical simulation performed in the PSIM simulation software. Its add-on module “Thermal module” was used to estimate semiconductor power losses using the datasheet parameters of the selected semiconductor devices. Results of calculations and simulation study were obtained for four operating points with different input voltage and constant input current to compare performance of the converters in renewable applications, like photovoltaic, where input voltage and power can vary significantly. Power loss breakdown is detailed and its dependence on the converter output power is analyzed. Recommendations are given for the use of the converter topologies in applications with low input voltage and relatively high input current.

Keywords – DC-DC power converters; Energy efficiency; Pulse width modulation converters; Semiconductor device modeling.

I. INTRODUCTION

Isolated full-bridge boost (IFBB) DC-DC converters are a well known and proven topology [1]–[5]. Up to recently, its spread is limited due to the inherent drawbacks of the current-fed technology, such as high inrush current during start-up and high voltage stress of the transistors. Nevertheless, the IFBB converters can perform voltage step-up and maintain continuous input current in a wide operation range. At the same time, a new quasi-Z-Source (qZS) DC-DC converter topology has emerged that has all the benefits of the IFBB topology and does not suffer from the high inrush current, has even higher step-up factor and therefore potentially wider operation range [6]–[8], [22], [23]. Therefore, the topologies with an input stage that can work as a current-source could be preferable in such low-voltage applications as power conditioners for photovoltaic panels and fuel-cells.

Focus in this paper is on the comparison of these two topologies in terms of energy efficiency in low voltage applications. The generalized power circuit layouts of the qZS and IFBB DC-DC converters are presented in Figs. 1 and 2.

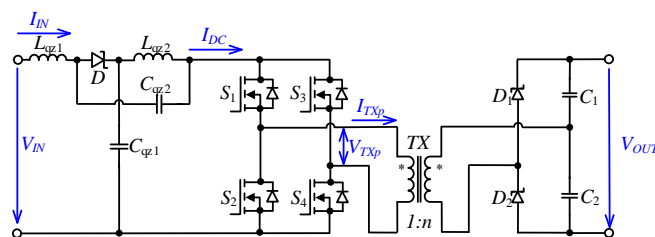


Fig. 1. Galvanically isolated qZS full-bridge DC-DC converter.

Both converters use the voltage doubler rectifier (VDR) to provide a higher voltage step-up factor and reduce the transformer turns ratio. The IFBB converter accommodates an active clamping circuit, which consists of a switch S_{CL} and a capacitor C_{CL} (Fig. 2). It is used to recycle the inductive energy when switching from the shoot-through to the active state, thus minimizing the turn-off losses and reducing the voltage stress of the switches.

II. OPERATION PRINCIPLE OF THE CONVERTERS

Fig. 3 shows the basic waveforms of the galvanically isolated qZS full-bridge DC-DC converter. The symmetric overlap of active states is used to control the converter in the continuous conduction mode (CCM). It requires generation of two control signals for the diagonal switches (one for S_1, S_4 and the other for S_2, S_3). These signals are of equal duration and phase-shifted by 180 degrees. The switching period consists of four time intervals:

- a) and c) are the shoot-through state intervals. All four inverter switches are conducting, qZS network inductors are accumulating energy;
- b) is an active state interval when diagonal switches S_1 and S_4 are conducting and energy is transferred to the output filter capacitor C_2 ;
- d) is another active state when diagonal switches S_2 and S_3 are turned on and energy is transferred to the output filter capacitor C_1 .

The operation principle of the qZS DC-DC converter is detailed in [8], [9].

The waveforms of the IFBB DC-DC converter are generalized in Fig. 4. The converter has an additional switch (S_{CL}), but in general the operation principle in the continuous conduction mode is similar to that of the qZS converter.

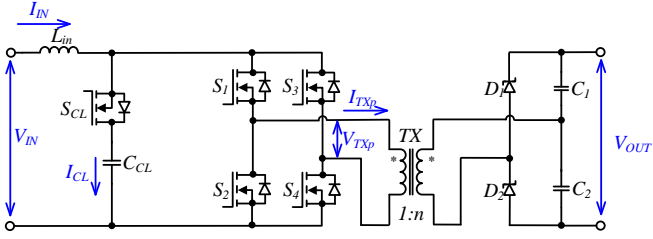


Fig. 2. Galvanically isolated full-bridge boost DC-DC converter.

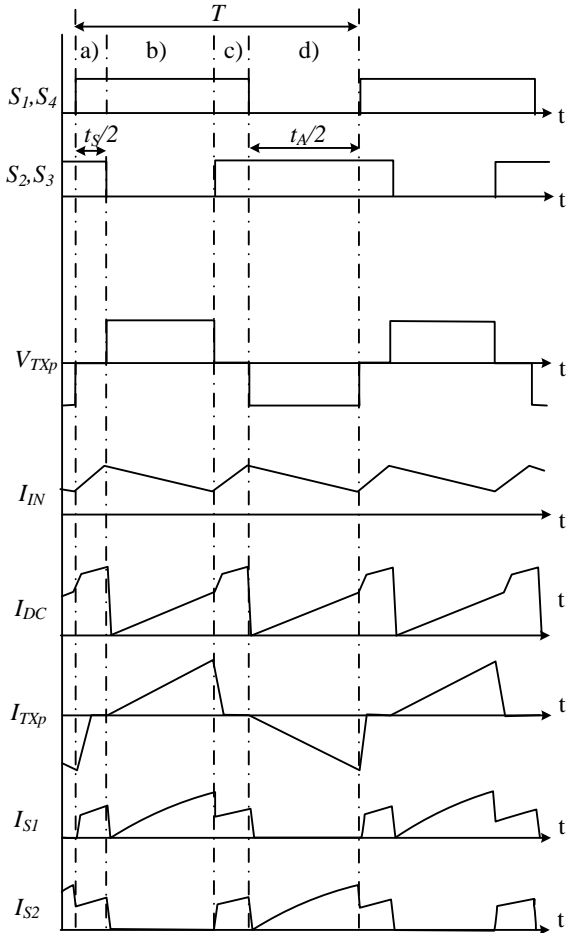


Fig. 3. Generalized waveforms of the qZS full-bridge DC-DC converter.

- a) and c) are the shoot-through intervals. All four inverter stage switches are conducting, the boost inductor L_{IN} is accumulating energy, the clamping switch S_{CL} is turned off;
- b) diagonal switches S_1 and S_4 are conducting, energy is transferred to the output filter capacitor C_2 , the clamping switch S_{CL} is turned on to protect inverter switches from the voltage overshoot during the transition from the shoot-through to the active state and back;
- d) diagonal switches S_2 and S_3 are conducting, energy is transferred to the output filter capacitor C_1 , the clamping switch S_{CL} is turned on to protect inverter switches from the voltage stress during the transition from the shoot-through to the active state and back.

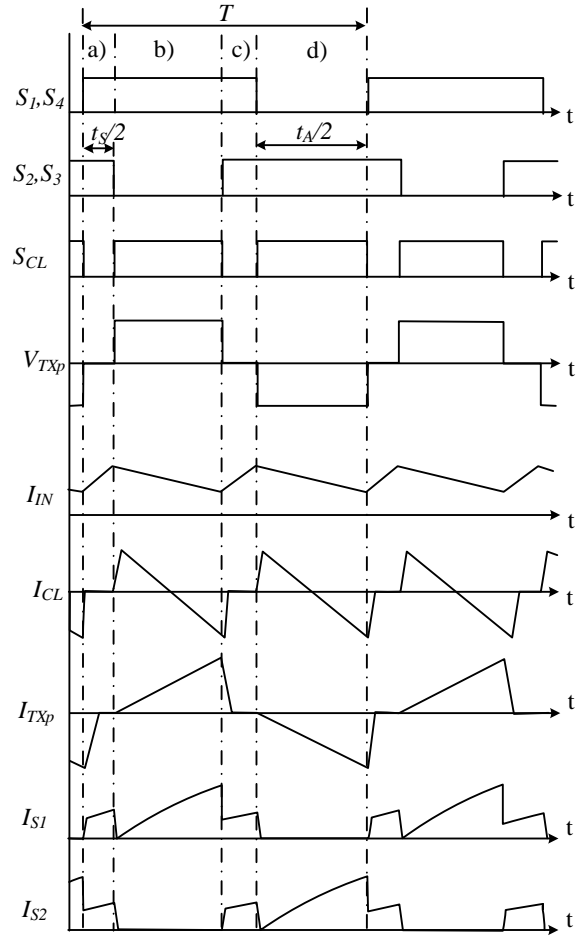


Fig. 4. Generalized waveforms of the IFBB DC-DC converter.

The operation principle of the IFBB DC-DC converter is detailed in [10], [11].

Comparison carried out in this paper is limited to the semiconductor losses because of their strong influence on the performance of both of the converters. To ensure reliable results, the converters were analyzed in the same conditions. Passive elements parameters were calculated to ensure the same input current ripple for both topologies. L_{IN} , L_{qz1} and L_{qz2} were selected to achieve peak-to-peak input current ripple at the level of 10 % of the nominal current.

As seen from Figs. 3 and 4, the current through the primary transformer winding (I_{TXp}) is nearly the same for both topologies. Thus, the losses in the magnetic elements have to be nearly equal for both converter topologies. They were excluded from our analysis, since the main difference in the power losses is within semiconductor losses.

III. DESIGN CONSIDERATION

Both of the compared topologies are boost-enabled, and their switching period T consists of the shoot-through and the active state. The duty cycles of the shoot-through and the active state are interdependent, as shown in (1):

$$\frac{t_A}{T} + \frac{t_S}{T} = D_A + D_S = 1, \quad (1)$$

where t_A and t_S are the duration of the active and the shoot-through state, correspondingly, D_A and D_S are the duty cycles of the active and the shoot-through state, correspondingly.

The output voltage of the qZS full-bridge converter can be expressed as

$$V_{OUT} = 2n \cdot \frac{1}{1 - 2D_S} \cdot V_{IN}, \quad (2)$$

where n is the transformer turns ratio, V_{IN} is the input voltage of the converter, and V_{OUT} is the output voltage of the converter. For the IFBB converter, the output voltage can be calculated as

$$V_{OUT} = 2n \cdot \frac{1}{1 - D_S} \cdot V_{IN}. \quad (3)$$

The main advantage of the discussed converters is the ability to operate with continuous input current. To maintain the CCM, the energy accumulating inductors must be selected based on the converter operation parameters.

For the IFBB converter, minimal inductance of the boost inductor required to limit the input current ripple on the level of $\Delta I\%$ can be calculated as [12]

$$L_{in} = \frac{V_{INmin}^2 \cdot D_{Smax}}{f_{SW} \cdot P \cdot \Delta I\%} \cdot 100, \quad (4)$$

where f_{SW} is the switching frequency, $\Delta I\%$ is the selected peak-to-peak input current ripple, D_{Smax} is the maximum shoot-through duty cycle, P is the rated power of the converter, and V_{INmin} is the minimum input voltage of the converter.

The inductance of the qZS network inductors required to limit the input current ripple on the level of $\Delta I\%$ from the nominal is expressed by [9]

$$L_{qz1} = L_{qz2} = \frac{1 - D_{Smax}}{1 - 2D_{Smax}} \cdot \frac{V_{INmin}^2 \cdot D_{Smax}}{f_{SW} \cdot P \cdot \Delta I\%} \cdot 100. \quad (5)$$

The capacitance of the capacitors in the qZS network required to limit the ripple of the DC-link voltage can be calculated as [13]:

$$C_{qz1} = C_{qz2} = \frac{2n \cdot P \cdot D_{Smax}}{V_{OUT} \cdot \Delta V\% \cdot V_{INmin} \cdot f_{SW}} \cdot 100, \quad (6)$$

where $\Delta V\%$ is the peak-to-peak voltage ripple of the capacitors.

To limit the output voltage ripple on the level of $\Delta V\%$, the capacitance of VDR capacitors should be at least [8]:

$$C_1 = C_2 = \frac{P \cdot D_{Smax}}{\Delta V\% \cdot f_{SW} \cdot V_{OUT}^2} \cdot 100, \quad (7)$$

where V_{OUT} is the nominal output voltage of the converter.

The capacitance of the clamping capacitor (C_{CL}) is based on the LC circuit resonant frequency. The clamping capacitor (C_{CL}) can resonate with either the boost inductor (L_{in}) or with the transformer leakage inductor (L_{TX_leak}). This resonant frequency should be lower than the doubled switching frequency f_{SW} . Since the IFBB converter circuit has two inductors, the clamping capacitance is calculated as the

maximum of two values, which is usually determined by L_{TX_leak} [14]:

$$C_{CL} = \frac{1}{16 \cdot L_{TX_leak} \cdot f_{SW}^2 \cdot \pi^2}. \quad (8)$$

IV. COMPARATIVE ANALYSIS OF POWER LOSSES AND EFFICIENCY

The semiconductor losses of the converter can be categorized to a few major types. Analytical expressions of semiconductor losses in both topologies are well described in [9], [11], [15]–[17]. Here some of the resulting expressions adapted for the discussed converters and applications are presented.

A. Inverter Losses

The primary low-voltage MOSFET semiconductor losses are calculated based on the MOSFET on-state resistance, the average input current, and transformer primary winding current averaged over on the half of the period. The use of average input current value instead of RMS value simplifies the analytical expressions for conduction losses during shoot-through state without significant impact on precision. For example, for the input current with ripple of 50 % the difference between average and RMS values is around 1 % only [17]. Conduction losses are different for the active and the shoot-through state as the different number of MOSFETs are conducting (Fig. 5). So the resulting equation consists of these two components. Total conduction losses in inverter MOSFETs of IFBB DC-DC converter are expressed by:

$$P_{Ms_con} = R_{DS(on)} \cdot \left(\frac{P}{V_{IN}} \right)^2 \cdot D_S + 2 \cdot R_{DS(on)} \cdot \left(\frac{4 \cdot n \cdot P}{\sqrt{3} \cdot V_{OUT}} \right)^2, \quad (9)$$

where $R_{DS(on)}$ is the on-state resistance of the MOSFET.

Total conduction losses in inverter MOSFETs of qZS DC-DC converter are expressed by:

$$P_{Ms_con} = R_{DS(on)} \cdot \left(\frac{2 \cdot P}{V_{IN}} \right)^2 \cdot D_S + 2 \cdot R_{DS(on)} \cdot \left(\frac{4 \cdot n \cdot P}{\sqrt{3} \cdot V_{OUT}} \right)^2, \quad (10)$$

As seen from (9) and (10) component of the inverter MOSFETs conduction losses that corresponds to the active state is the same for both topologies as the difference in RMS values of the transformer primary winding current is compensated by difference in duty cycles of the active state. At constant input current (P/V_{IN}), the MOSFET current during the shoot-through state interval is two times higher in qZS converter than in IFBB converter. However, the shoot-through duty cycle (D_S) for qZS converter is two times lower than for IFBB converter. Therefore component of the inverter

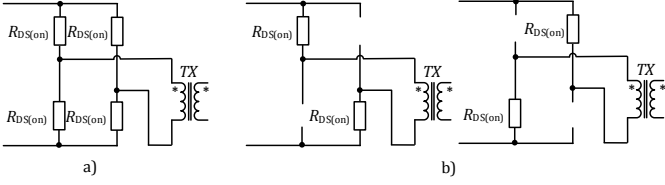


Fig. 5. Equivalent scheme of the inverter during the shoot-through (a) and the active (b) state.

MOSFETs conduction losses that corresponds to the shoot-through state is only two times higher than in IFBB converter. Impact of this component decreases as the shoot-through duty cycle decreases and thus inverter MOSFETs conduction losses are equal for both converters at unity step-up factor.

Switching losses consist of turn-on and turn-off losses:

$$P_{M_sw} = 4 \cdot (P_{M_on} + P_{M_off}), \quad (11)$$

where P_{M_on} and P_{M_off} are the MOSFET turn-on and turn-off losses accordingly [19]:

$$P_{M_on} = \frac{1}{2} \cdot \alpha \cdot (I_{IN} - I_{IN} \cdot \Delta I_{\%} / 200) \cdot \frac{V_{out}}{2n} \times \left(\frac{Q_{SW}}{V_{drive}} \cdot (R_g + R_{drive}) \right) \cdot f_{SW}, \quad (12)$$

where I_{IN} is the converter input current, Q_{SW} is the MOSFET switching charge, V_{drive} is the MOSFET driver logical “high” voltage (15 V), R_g is the MOSFET internal gate resistance, R_{drive} is the MOSFET driver current limiting resistor (2 Ω);

$$P_{M_off} = \frac{1}{2} \cdot \alpha \cdot (I_{IN} + I_{IN} \cdot \Delta I_{\%} / 200) \cdot \frac{V_{out}}{2n} \times \left(\frac{Q_{SW}}{V_{drive}} \cdot (R_g + R_{drive}) \right) \cdot f_{SW}, \quad (13)$$

In both equations (12)–(13) the coefficient α is used to take into account difference between MOSFET current in shoot-through state in the qZS and IFBB converters. In the worth case, when all switching transients are hard, the inverter MOSFET switching losses differs by two times, since $\alpha = 0.5$ for IFBB converter and $\alpha = 1$ for qZS converter. At constant input current, the switching losses of the inverter MOSFETs do not depend on the duty cycle and are fully determined by the parameters of the MOSFETs and the isolation transformer.

B. VDR Losses

The conduction losses of VDR diodes could be estimated by [20]

$$P_{VDR_con} = 2 \cdot \left(V_{FV_Vrect} \cdot \frac{P}{V_{OUT}} \right), \quad (14)$$

where V_{FV_Vrect} is the forward voltage drop of the VDR diode.

As seen from (14), conduction losses are growing with the output power.

C. Power Losses in the qZS Diode

Since the diode is used in the qZS network, the conduction losses depend only on its average current [18], [19]:

$$P_{DqZS_con} = V_{FV_DqZS} \cdot I_{IN}, \quad (15)$$

where V_{FV_DqZS} is the forward voltage drop of the qZS diode.

Conduction losses of the qZS diode depend on the shoot-through duty cycle. Taking into account the change of D_S in the range of 0...0.25 (for the converter operating with the twofold input voltage range), the conduction losses will change roughly only by 6%.

D. Losses in Clamping MOSFET

Total power losses on the clamping switch consist of three components:

$$P_{CL} = P_{CL_con} + P_{CL_on} + P_{CL_off}, \quad (16)$$

where P_{CL_con} is the clamping switch conduction losses, P_{CL_on} and P_{CL_off} are the clamping MOSFET turn-on and turn-off losses [11], [16]:

$$P_{CL_con} = \frac{R_{DS(on)} \cdot I_{IN}^2}{2} \cdot (1 - D_S), \quad (17)$$

$$P_{M_on} = \frac{1}{2} \cdot (I_{IN} - I_{IN} \cdot \Delta I_{\%} / 200) \cdot \frac{V_{out}}{2n} \times \left(\frac{Q_{SW}}{V_{drive}} \cdot (R_g + R_{drive}) \right) \cdot f_{SW}, \quad (18)$$

$$P_{M_off} = \frac{1}{2} \cdot (I_{IN} + I_{IN} \cdot \Delta I_{\%} / 200) \cdot \frac{V_{out}}{2n} \times \left(\frac{Q_{SW}}{V_{drive}} \cdot (R_g + R_{drive}) \right) \cdot f_{SW}. \quad (19)$$

Equations (17)–(19) indicate that only conduction losses depend on the shoot-through duty cycle. So, at constant input current, the total losses of the clamping switch will be growing, moving toward the unity step-up factor ($D_S = 0$).

V. SIMULATION RESULTS

The 300 W solar module-integrated converter (MIC) was selected as the case study for the modeling. Typically MICs working with a single PV-panel have the nominal output power in the range 240–275 W and maximum power point voltage near 30 V at standard test conditions. The converter parameters must be within that range. The simulation parameters of the converters are listed in Table I.

The power losses and efficiency of both converters were analyzed in four operating points, which cover the whole input voltage range (Table II). The operation parameters of each point were selected to achieve the maximum input current. As seen from Table II and (2), (3), the shoot-through duty cycle D_S needed to achieve the desired voltage boost factor is two times smaller for the qZS converter as compared to the IFBB converter counterpart. This has considerable influence on the distribution of the losses in the converters.

The power loss was analyzed by means of the PSIM simulation software with Thermal Module. It enables the calculation of the power loss in the semiconductor elements based on their datasheet parameters. The semiconductor

elements selected for the simulation and their main parameters are presented in Table III.

To compare simulation and theoretical results, the losses calculated using (9)–(19) are shown in Tables IV and V for qZS and IFBB converters, respectively. The IFBB converter shows up to 4.7 % higher calculated efficiency in boost mode.

The simulation results are presented in Tables VI and VII for qZS and IFBB converters, respectively. Fig. 6 shows the graphical representation of the semiconductor losses for both topologies. The dependence of semiconductor losses on the

TABLE I

PARAMETERS OF THE COMPARED DC-DC CONVERTERS

Parameter	Symbol	Value
Input voltage range, V	V_{IN}	15...30
Maximum input current, A	I_{IN}	10
Output voltage, V	V_{OUT}	300
Switching frequency, kHz	f_{SW}	100
Transformer turns ratio	n	5
Capacitance of output capacitors, μF	C_1, C_2	2.2
Converters power rating, W	P	300
Peak-to-peak input current ripple, %	$\Delta I_{\%}$	10
Peak-to-peak voltages ripple, %	$\Delta V_{\%}$	1
Transformer magnetizing inductance, μH	L_{TX_m}	60
Transformer primary leakage ind., μH	$L_{TX_{leak}}$	0.38
qZS converter		
Capacitance of qZS capacitors, μF	C_{qz1}, C_{qz2}	33
Inductance of qZS inductors, μH	L_{qz1}, L_{qz2}	28
IFBB converter		
Inductance of boost inductor, μH	L_{in}	38
Capacitance of clamping capacitor, μF	C_{CL}	17

TABLE II

INPUT VOLTAGE AND POWER IN THE SELECTED OPERATING POINTS

Operating point	1	2	3	4
V_{IN} , V	15	20	25	30
P , W	150	200	250	300
$D_{S_{qZS}}$	0.25	0.167	0.083	0
$D_{S_{IFBB}}$	0.5	0.333	0.167	0

TABLE III

SEMICONDUCTOR COMPONENTS SELECTED FOR THE SIMULATION

Component	Type	Specifications
$S_1...S_4, S_{CL}$	Vishay Si4190ADY	$V_{DS} = 100 \text{ V}$, $R_{DS(on)} = 8.8 \text{ m}\Omega$, $I_D = 18.4 \text{ A}$, $C_{OSS} = 695 \text{ pF}$, $R_g = 1.1 \Omega$, $Q_g = 67 \text{ nC}$
D	Vishay V60D100C	$V_{RRM} = 100 \text{ V}$, $V_F = 0.66 \text{ V}$, $I_F = 2 \times 30 \text{ A}$
D_1, D_2	CREE C3D02060E	$V_{RRM} = 600 \text{ V}$, $V_F = 1.8 \text{ V}$, $I_F = 4 \text{ A}$

TABLE IV

CALCULATED POWER LOSSES OF THE QZS CONVERTER

	Output power, W			
	150	200	250	300
qZS diode (cond.), W	6.60	6.60	6.60	6.60
MOSFETs (cond.), W	1.47	1.63	1.92	2.35
MOSFETs (switch), W	1.10	1.10	1.10	1.10
Rectifier diodes (cond.), W	1.80	2.40	3.00	3.60
Total losses, W	10.97	11.73	12.62	13.65
Efficiency, %	92.7	94.1	95.0	95.5

TABLE V

CALCULATED POWER LOSSES OF THE IFBB CONVERTER

	Output power, W			
	150	200	250	300
Clamping MOSFET, W	0.50	0.57	0.64	0.72
MOSFETs (cond.), W	1.03	1.34	1.78	2.35
MOSFETs (switch), W	0.55	0.55	0.55	0.55
Rectifier diodes (cond.), W	1.80	2.40	3.00	3.60
Total losses, W	3.87	4.86	5.97	7.21
Efficiency, %	97.4	97.6	97.6	97.6

output power for the qZS and IFBB converters are shown in Figs. 7 and 8, respectively. In both converters the contribution of switching losses of the MOSFETs to the total losses remains nearly the same for the whole operation range. The IFBB converter has lower switching losses due to the clamping network that brings inverter stage MOSFET operation mode to partial soft-switching at higher loads.

It is observed that in the qZS converters the main contributor of losses is the qZS diode. It generates more than 50 % of the total losses in the entire operation range. As the power increases, the conduction losses on the qZS diode are decreasing due to the minimization of the input current ripple in the operating point with the unity step-up factor.

The second main source of losses in the qZS and the main one in the IFBB converter is the conduction losses of the VDR diodes. In both cases they are increasing almost linearly along with the output power increase. This is due to the increase of the output current while the rectifier diodes forward voltage drop remains nearly constant. In the point with the unity step-up factor, the VDR conduction losses are equal for both topologies as they are working with the same output current

TABLE VI

SIMULATED POWER LOSSES OF THE QZS CONVERTER

	Output power, W			
	150	200	250	300
qZS diode (cond.), W	6.45	6.31	6.28	6.24
MOSFETs (cond.), W	1.98	2.07	2.37	2.50
MOSFETs (switch), W	0.39	0.39	0.37	0.49
Rectifier diodes (cond.), W	1.39	1.99	2.60	3.30
Total losses, W	10.21	10.76	11.62	12.53
Efficiency, %	93.2	94.6	95.4	95.8

TABLE VII

SIMULATED POWER LOSSES OF THE IFBB CONVERTER

	Output power, W			
	150	200	250	300
Clamping MOSFET, W	0.41	0.44	0.48	0.52
MOSFETs (cond.), W	1.70	1.94	2.22	2.49
MOSFETs (switch), W	0.29	0.25	0.21	0.20
Rectifier diodes (cond.), W	1.69	2.24	2.78	3.34
Total losses, W	4.09	4.87	5.69	6.55
Efficiency, %	97.3	97.6	97.7	97.8

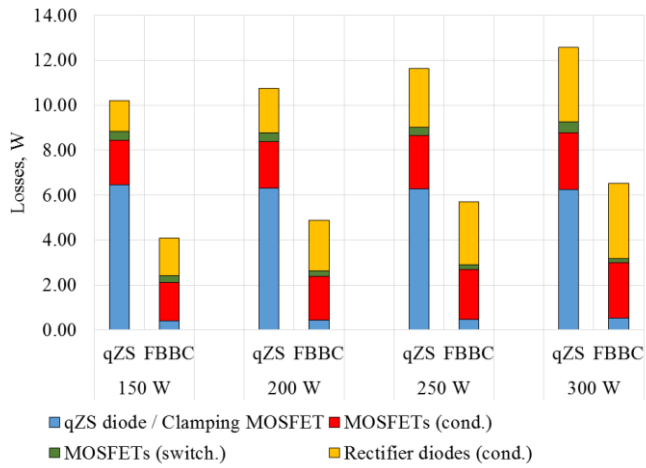


Fig. 6. Semiconductor power losses breakdown of the qZS and IFBB converters.

and duty cycle. At the same time, in other operating modes the VDR losses in the qZS topology are lower than in the IFBB topology. The reason is that to provide the same average output current with a lower active state duty cycle, the VDR diode peak current in the IFBB converter must be higher.

In the IFBB converter, the D_A increases with the output power growing. Therefore, the losses in the clamping MOSFET are rising, since it is conducting only during the active state. In general, the direct impact of the clamping MOSFET losses on the converter efficiency is insignificant.

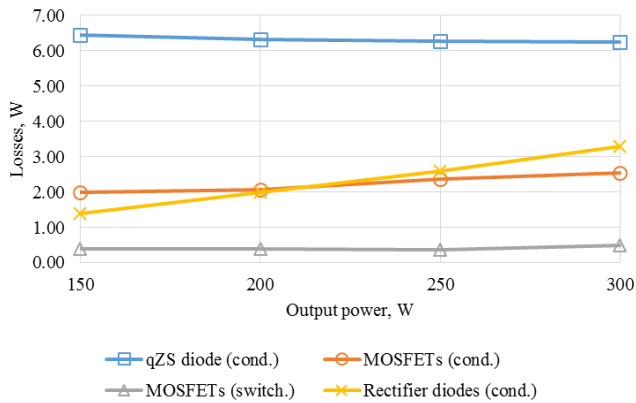


Fig. 7. Semiconductor power losses versus output power in the qZS converter.

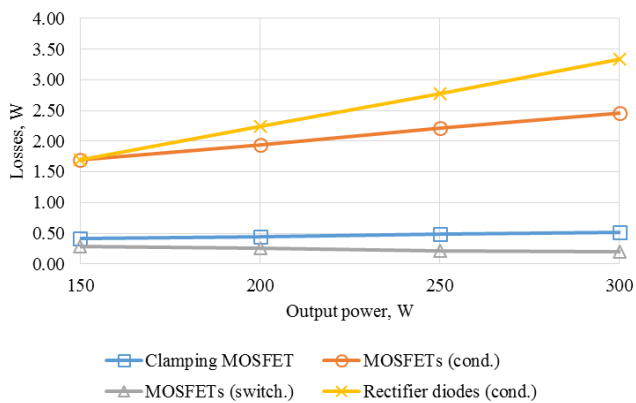


Fig. 8. Semiconductor power losses versus output power in the IFBB converter.

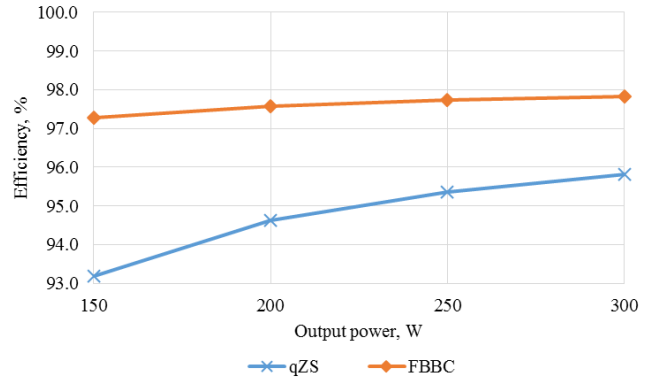


Fig. 9. Efficiency of qZS and IFBB converters versus output power.

Nevertheless, the clamping network has substantial impact on the inverter MOSFET switching losses [10], [15].

The switching losses of the inverter MOSFETs in qZS converter are higher than that in the IFBB converter. It is a result of the higher switching current in boost mode for qZS, as predicted by (12)–(13), and soft-switching possibilities of the IFBB converter with active clamping [24]. This soft-switching performs better at higher load and leads to lower switching losses of the inverter MOSFETs.

The last component in the power losses is the MOSFET conduction losses. They are increasing with the output power increase due to the higher power losses during active state, which depend on the load. In the active state, two MOSFETs are connected in series with the transformer primary winding and conducting output current reflected to the primary winding of the isolation transformer. With given test conditions for both converter topologies the RMS current of the inverter MOSFETs during active state interval differs in boost mode. However they feature equal conduction losses in active state, since different in RMS currents is compensated by the difference of active state duty cycles. The difference in total conduction losses of the inverter MOSFETs for these two converters is determined by the losses during shoot-through state. As shown in Fig. 5, in the shoot-through state the input current is flowing through the parallel connection of two branches with two conducting MOSFETs connected in series [7]. For the IFBB converter in the shoot-through state, the RMS current through each inverter MOSFET is equal to half of the average input current. In the qZS converter the RMS MOSFET current equals to the average input current. Consequently, the conduction losses during shoot-through state in the inverter MOSFETs of the qZS converter are two times higher than that of the IFBB converter, taking into account two times higher duty cycle required for IFBB converter to achieve the same voltage step-up as in the qZS converter. In both converters the conduction losses during the shoot-through state are proportional to its duty cycle. Therefore their impact growing as the step-up factor increases, i.e. the converter input voltage decreases. Since the difference in the conduction losses between two converters is determined only by the component caused from the shoot-through state, the inverter MOSFETs conduction losses are equal for both

topologies in the operating point with the unity step-up factor, which was confirmed by the simulation.

The dependences of the efficiency on the output power for both converters are summarized in Fig. 9. As can be seen, the efficiency curve of the IFBB converter is flat over the whole operation range, while the qZS converter efficiency drops significantly with the decrease of the output power. This efficiency drop is caused mainly by the nearly constant qZS diode conduction losses. They have a crucial impact on the efficiency at light loads.

In general, the distribution of the losses and their dependence on the output power corresponds to the analytical expressions in section III of this paper.

VI. CONCLUSION

In this paper the semiconductor losses in the isolated qZS and IFBB converters were analyzed and compared.

The comparison shows that the IFBB DC-DC converter topology could be more preferable in low-voltage applications than the conventional qZS full-bridge converter topology with a diode in the qZS network. At the same time, the IFBB converter topology has a number of drawbacks that limit its use. Major drawbacks are the high inrush current and higher voltage stresses under hard-switching as compared to the qZS and conventional voltage fed topologies. Additional active clamping circuit is commonly used in the IFBB converters to improve their switching performance.

Nevertheless, both topologies can be significantly improved in terms of efficiency. For example, by accommodating synchronous qZS-network and synchronous rectification it is possible to increase the maximum efficiency of the qZS converter by up to 3 % [7]. This eliminates the main drawback of the qZS converter in low voltage applications. By accommodating separated commutation and four quadrant active switches to the IFBB converter, it is possible to limit voltage stress by achieving full soft-switching and to minimize rectifier stage conduction losses by the use of synchronous rectification [4], [20].

Efficiency is not a single factor in topology selection for low voltage applications. The following additional points for consideration have resulted from our comparison of the discussed topologies in terms of practical applications:

- 1) qZS converters need fewer MOSFETs, which provides cost savings on MOSFETs themselves, driver circuits, and control system.
- 2) IFBB converters have only one energy-accumulating inductor as compared to two inductors in the qZS topology. At the same time, the inductance of the IFBB converter inductor is higher than the inductance of the qZS inductors. Moreover, the qZS network inductors can be magnetically coupled, which allows the required inductance value to be reduced two times in the same operating conditions [13], [21]. It means that the qZS can be implemented with a single magnetic component like the IFBB converter.
- 3) qZS DC-DC converters can work in both the shoot-through and the open state of the inverter, while the

IFBB converter needs special circuits and more complex control algorithms to protect the inverter from the voltage overshoot caused by the boost inductor if the open state occurs in the inverter bridge.

- 4) qZS DC-DC converters have comparatively low efficiency in low voltage applications but can additionally operate in the buck mode (without any additional switches), providing a wider operation range without any need for clamping circuits to protect switches from the voltage stress.
- 5) qZS DC-DC converters have higher step-up factor (up to 3 with an acceptable level of MOSFET conduction losses), which extends the operating range as compared to that of the IFBB converter [7].

By adopting modern control algorithms and semiconductor devices, current fed topologies have all chances to become widespread in low voltage applications, especially those requiring continuous input current. The choice of a particular topology is determined by the specific application and the additional requirements to the converter.

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