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# Asymmetric Snubberless Current-Fed Full-Bridge Isolated DC-DC Converters

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***Abstract* – This paper presents two isolated current-fed full-bridge DC-DC converters that can be used to interface a lower voltage source into a DC bus of higher voltage. The first topology uses a resonant circuit to force current redistribution between low-voltage-side transistors and a passive rectifier. The second topology utilizes an active rectifier with secondary modulation to achieve the same goal. The resonant circuit can be formed by using transformer leakage inductance and the parasitic capacitances of the switches. The converters feature soft switching of semiconductors over a wide range of operating conditions. This is achieved with decreased energy circulation when compared to existing topologies with symmetric control and with fewer semiconductors than in those with phase-shift control. The topologies can be implemented in renewable, supercapacitor, battery, fuel cell, and DC microgrid applications. Steady-state operation and design aspects of the converters are presented and verified experimentally with 400 W prototypes.**

***Keywords* – DC-DC power converters; Soft switching; Zero-current switching; Zero-voltage switching.**

## I. Introduction

Power electronic systems with a variable gain are required to interface different renewable energy sources or storage systems into the microgrid [1]. Converters with transformers are often preferred due to reduced stresses on the components and better flexibility of application [2], [3]. A significant portion of the past and present research that is related to isolated DC-DC converters is focused on voltage-fed dual-active-bridge (DAB) topologies [4]–[6]. These converters feature good regulation capabilities and soft switching over a wide range of operating conditions with advanced multi-mode digital control algorithms. At the same time, isolated current-fed (CF) converters could be beneficial due to their inherent boost capability, low input current ripple, reduced energy circulation, reduced requirements regarding the isolation transformer and simpler control system [7]–[9]. The present study is focused on full-bridge-type topologies due to their flexibility and scalability, making them suitable for a wide range of applications with various voltage and power levels. A common drawback of isolated CF topologies is related to voltage overshoots across primary transistors due to the leakage inductance of practical transformers. This issue is usually solved by applying a RCD snubber [10], the active clamp circuit introduced in [11] or solutions without snubbers, by utilizing the parasitic parameters of the circuit [14]–[17]. The latter approach is advantageous due to the reduced number of components required and the soft switching provided for power switches in the topology.

Existing snubberless (also referred to as “clampless”) converters can utilize the symmetric [12], [13] control algorithm or the phase-shift one [14]–[17]. In phase shift control, the primary switches need to have the reverse-blocking capability. Given the typical realization of this function (with a series diode or an anti-series switch), it leads to a remarkable increase in the total number of primary semiconductors and their power losses. On the other hand, at some operating points, symmetric topologies have excessive energy circulation and increased current stress on the primary switches and the transformer. In addition to the existing solutions, the present paper proposes two asymmetric topologies that combine the properties of both approaches and could provide an improved weighted performance, particularly if the converters have to operate under a wide range of input voltage and power levels. In this paper, operation with a full-bridge rectifier is assumed; however, the voltage-doubler rectifier can be applied for both converters as well. The operation principle of the topologies is described in Section II, design guidelines are presented in Section III and the experimental results are demonstrated in Section IV.

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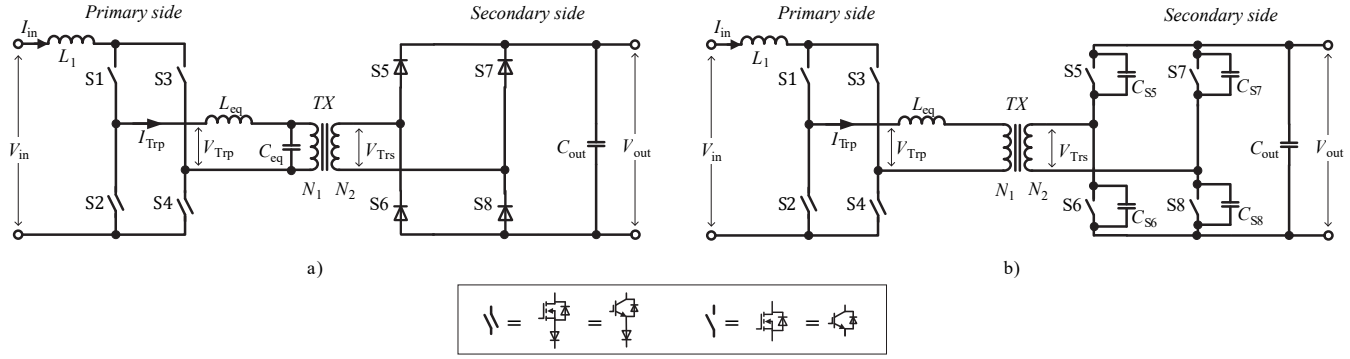


Fig. 1. Topology of the asymmetric converters proposed: ARPC (a), ASMB (b).

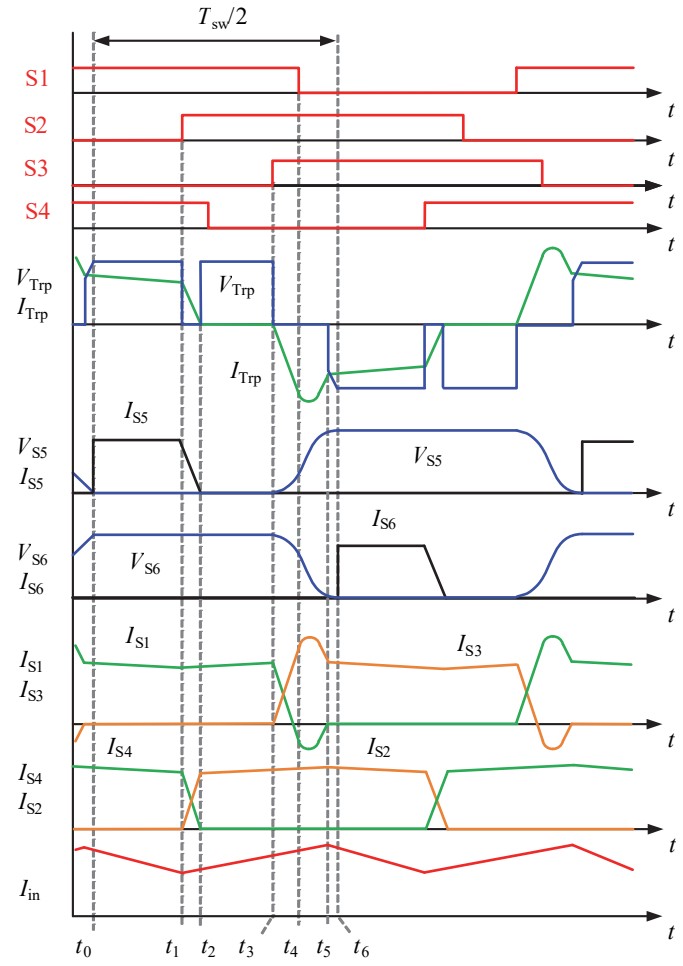


Fig. 2. Idealized operating waveforms of APRC with a passive rectifier.

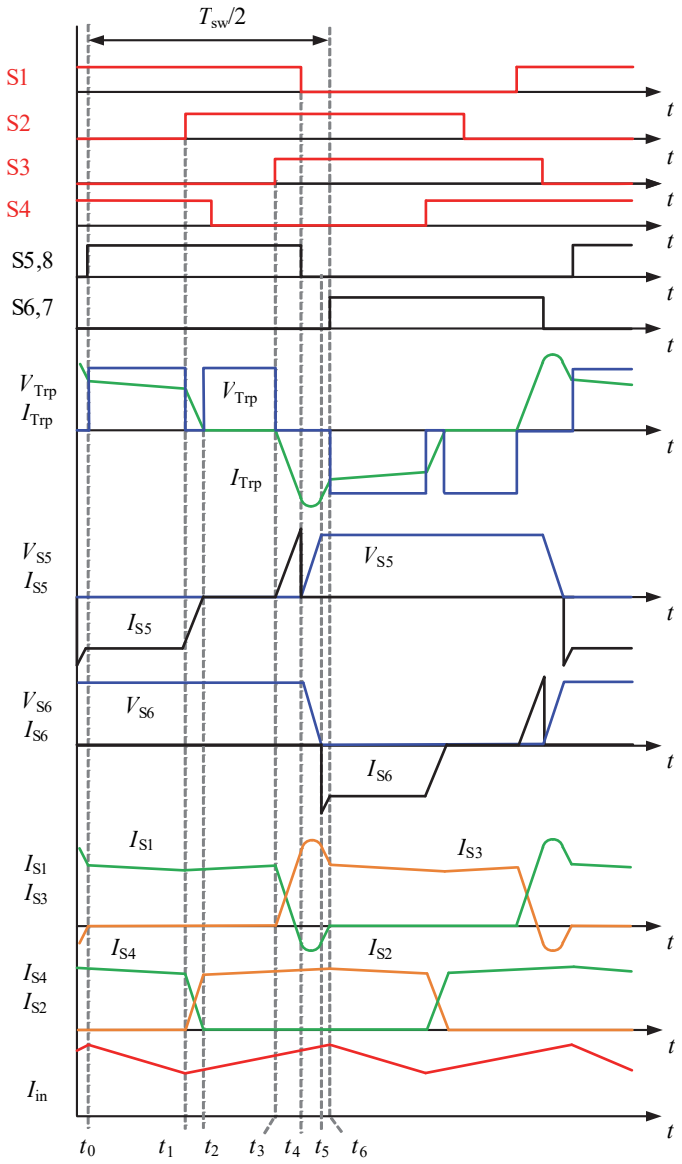


Fig. 3. Idealized operating waveforms of ASMC with an active rectifier.

## II. Description of Operation

The converter topologies proposed are shown in Fig. 1. As can be observed, they feature two reverse-conducting and two reverse-blocking devices at the primary side. The asymmetric parallel resonant converter (APRC) topology can be implemented with a passive rectifier (Fig. 1a). It utilizes a resonant tank formed by $L_{eq}$ and $C_{eq}$ to redistribute current between the top transistors. The asymmetric secondary modulation-based converter (ASMC) topology in Fig. 1b has an active rectifier that is used to force the currents to change direction and achieve the same goal. The equivalent capacitor across the transformer primary winding can be formed by the intrinsic capacitances of the rectifier switches ($C_{S5}$–$C_{S8}$) and/or separately. Similarly, the equivalent inductance can represent the leakage inductance of the transformer reflected to the primary winding or by an additional inductor in series to the primary winding. Both topologies operate at a constant switching frequency and regulate output voltage by phase-shift between the top and bottom switches. The operation of the converters presented in Figs. 2 and 3 can be described by six switching modes for each half-period $T_{sw}/2$.

### *A. The APRC Topology*

$t_0$–$t_1$: switches S1 and S4 are turned on and the other ones are turned off. The converter is in the active state and the power is transferred to the output through switches S1, S4 and diodes S5 and S8. At the end of this interval, the input current reaches the minimum value.

$t_1$–$t_2$: S2 is turned off and the active state is finished. The current of S2 rises, while the current of S4 decreases linearly with d$i$/d$t$, caused by the equivalent leakage inductance. The currents of S5 and S8 as well as the transformer current decrease with the same slope. The input inductor voltage polarity is reversed and its current starts to increase, while the transformer primary voltage is zero.

$t_2$–$t_3$: the current of S2 reaches the input current level and the transformer primary voltage rises to the amplitude value. The converter is in the shoot-through state with S1 and S2 conducting while the input inductor is energized. S4 could be turned off with ZCS.

$t_3$–$t_4$: S3 is turned on and the resonant process is started. Capacitor $C_{eq}$ starts to recharge and, as a result, the S1 current decreases and the S3 current increases (Fig. 2).

$t_4$–$t_5$: when the resonant current becomes higher than the input current, the soft switching condition is satisfied; the body diode of S1 starts to conduct and the transistor channel can be turned off with ZCS. The currents at the primary side reach the amplitude value when the capacitor voltage crosses zero and, as the capacitor $C_{eq}$ voltage polarity changes, starts to decrease back to the value of the input current.

$t_5$–$t_6$: the currents at the input side are equal to the input current and the recharging of capacitor $C_{eq}$ continues. When $C_{eq}$ and the transformer voltages reach the amplitude value, rectifier switches S6 and S7 become forward-biased and start to supply the current to the output. From $t_6$ the converter active state starts and the processes are then repeated for another switching half-period.

### *B. The ASMC Topology*

The first three modes are equivalent to those in APRC.

$t_0$–$t_1$: switches S1 and S4 are turned on and the other ones are turned off. The converter is in the active state and the power is transferred to the output through switches S1, S4 and MOSFETs S5 and S8. At the end of this interval, the input current reaches the minimum value.

$t_1$–$t_2$: S2 is turned off and the active state is finished. The current of S2 rises, while the current of S4 decreases linearly with d$i$/d$t$, caused by the equivalent leakage inductance. The currents of S5 and S8 as well as the transformer current decrease with the same slope. The input inductor voltage polarity is reversed and its current starts to increase, while the transformer primary voltage is zero.

$t_2$–$t_3$: the current of S2 reaches the input current level and the transformer primary voltage rises to the amplitude value. The converter is in the shoot-through state with S1 and S2 conducting while the input inductor is energized. S4 could be turned off with ZCS.

$t_3$–$t_4$: S3 is turned on and the current of S3 rises, while the current of S1 decreases linearly with d$i$/d$t$, caused by equivalent leakage inductance. This mode is analogous to the interval $t_1$–$t_2$ (Fig. 3).

$t_4$–$t_5$: since S1 is a reverse-conducting device, after decreasing to zero, the current starts to flow through its body diode, changing with the same slope, while the current through S3 rises above the input current. Thus, the soft switching condition is satisfied and S1 can be turned off with ZCS, along with S5 and S8. The equivalent capacitor recharges and the transformer voltage changes its polarity.

$t_5$–$t_6$: capacitor $C_{eq}$ is recharged, the transformer secondary voltage reaches the amplitude value and the body diodes of S6 and S7 become forward-biased. The current through S1 returns back to zero with the same d$i$/d$t$, and the current of S3 and the transformer primary current become equal to the input current. From $t_6$, the converter active state is started, hence S6 and S7 can be turned on to avoid excessive losses in the body diodes. The processes are then repeated for another switching half-period.

### *C. Design Aspects*

#### *1. The APRC converter*

For APRC, soft switching is achieved if peak transformer primary current $I_{P(res)}$ is larger than input inductor current $I_{in}$.

$$I_{P(res)} = \frac{V_{out}}{nZ_r} \geq I_{in}, \tag{1}$$

where $V_{out}$ is the output voltage, $n$ is the transformer turns ratio and $Z_r$ is the impedance of the resonant circuit:

$$Z_r = \sqrt{\frac{L_{eq}}{C_{eq}}}, \tag{2}$$

where $L_{eq}$ is the inductance of the equivalent circuit (largely determined by transformer leakage inductance) and $C_{eq}$ is the equivalent capacitance, which can be represented by the intrinsic capacitance of the rectifier semiconductor and/or an external capacitor.

To satisfy the soft switching criteria for a wide range of conditions, the resonant circuit should be designed around minimal input voltage at full load. The required impedance of the resonant tank $Z_r$, should be chosen according to

$$Z_r = \sqrt{\frac{L_{eq}}{C_{eq}}} \le \frac{V_{out}}{nI_{P(res)}} = \frac{V_{in(min)}V_{out}}{nP_{max}}, \quad (3)$$

where $P_{max}$ is the maximum power of the converter. The required resonant frequency is estimated by

$$f_r = \frac{f_{sw}}{1-\frac{n}{G_{min}}}, \quad (4)$$

where $f_{sw}$ is the converter switching frequency and $G_{min}$ is the desired minimum converter voltage gain. The resonant frequency is calculated from

$$f_r = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}}. \quad (5)$$

From (3)–(5), the equation for the required equivalent inductance $L_{eq}$ is obtained from

$$L_{eq} = \frac{Z_r}{2\pi f_r}. \quad (6)$$

The associated resonant capacitance can then be derived from (3).

The duty cycle of the switches should be higher than 0.5 to avoid open circuit of the input inductor and for S2 and S4, it can be approximated as

$$D_{S2,S4}^{min} \ge \frac{1}{2} + \frac{nL_{eq}P_{max}}{V_{in}V_{out}}. \quad (7)$$

For the other pair of switches (S1 and S3), the required duty cycle is estimated from

$$D_{S1,S3} = \frac{1}{2} + \frac{f_{sw}}{4f_r}. \quad (8)$$

The gain of this converter is not sensitive to load variations and is estimated from

$$G = \frac{n}{1-f_{sw}\left(\frac{1}{f_r}+2t_{2-3}\right)}. \quad (9)$$

*2. The ASMB Converter*

For the ASMB converter, the duty cycle of the switches can be calculated from (8) for the minimum possible input voltage and the maximum power level. It should be noticed that a longer duty cycle would lead to an increased peak current at the primary side and excessive energy circulation. In the ideal case, the peak current of the converter should be equal to maximum possible input current $I_{in(max)}$, and the switch duty cycle is obtained by

$$D = \frac{1}{2} + \frac{nI_{in(max)}L_{eq}f_{sw}}{V_{out}}, \quad (10)$$

where $I_{in(max)} = P_{max}/V_{in(min)}$.

The minimum total duration of the shoot-through state ($t_1$–$t_6$) is then estimated from

$$t_{1-6(min)} = \frac{2\left[L_{eq}\left(nI_{in(max)}\right)^2 + C_{eq}V_{out}^2\right]}{nI_{in(max)}V_{out}}. \quad (11)$$

As shown, both $L_{eq}$ and $C_{eq}$ increase the resulting minimum duration of the shoot-through state. Therefore, they should be carefully selected to have the desired regulation capabilities of the converter. The converter gain can be then estimated from

$$G = \frac{1}{1-2f_{sw}\left(t_{2-3}+t_{1-6(min)}\right)}. \quad (12)$$

*3. Generalizations*

Unlike in other topologies with phase shift control, the peak current of the top transistors is higher than the input current, which offers a specific advantage. From the operational waveforms and equations presented it follows that the recharging of capacitor $C_{eq}$ takes place when the current is at its peak value, which is higher than the maximum input current. Thus, the capacitor recharge time is constant and unaffected by the converter operating point and operation at light load does not affect converter gain or require adjustments to the control strategy. Since only top transistors exhibit such an increased current, the total energy circulation through semiconductors at low-load conditions can be lower than that of the topologies with symmetric control. While the APRC topology requires lesser number of active switches, the ASMB provides a larger degree of freedom when choosing the value of $C_{eq}$. Moreover, if the input current value is known, the implementation of digital control to adjust the duty cycles of the switches would allow a significant reduction of the circulating energy.

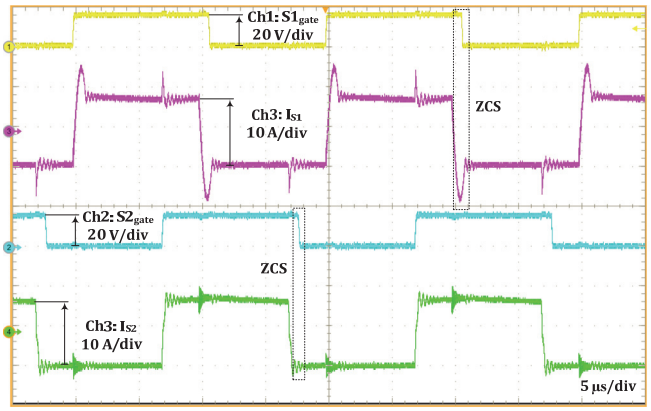


Fig. 4. Experimental waveforms of an APRC converter: Ch1 – S1 gate voltage, Ch2 – S2 gate voltage, Ch3 – S1 current and Ch4 – S2 current.

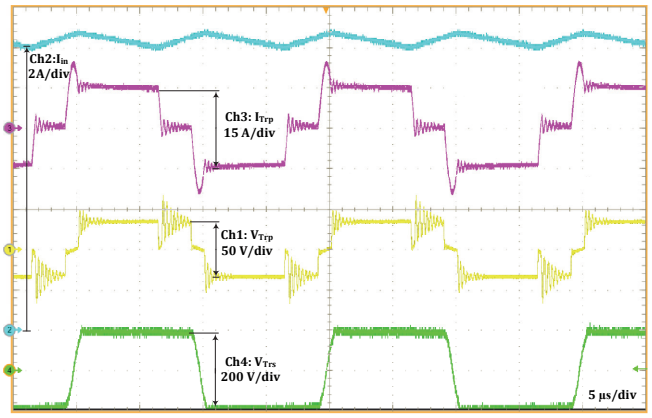


Fig. 5. Experimental waveforms of an APRC converter: Ch1 – $V_{Trp}$, Ch2 – $I_{in}$, Ch3 – $I_{Trp}$ and Ch4 – $V_{Trs}$.

## III. Experimental Verification

To validate the proposed converters, an experimental prototype with a rated power of 400 W was assembled and both topologies were tested with the same hardware. Synchronous MOSFETs instead of series diodes were applied in the primary part to reduce conduction losses. The parameters and components used are listed in Table I.

TABLE I

Parameters and Components of the Experimental Prototype

| Parameter/component | Symbol | Value |
|---|---|---|
| Input voltage, DC | $V_{in}$ | 20–30 V |
| Output voltage, DC | $V_{out}$ | 400 V |
| Switching frequency | $f_{sw}$ | 50 kHz |
| Primary side inductors inductance | $L_1$ | 100 µH |
| Equivalent capacitance (at TX primary winding) | $C_{eq}$ | 10 nF |
| Transformer turns ratio | $N_2/N_1$ | 13 : 1 |
| Equivalent TX leakage inductance | $L_{eq}$ | 0.8 µH |
| Rated power | $P_{rated}$ | 400 W |
| Primary-side transistors | S1–S4 | FDMS86181 |
| Secondary-side transistors | S5–S8 | STP18N60DM2 |
| Microcontroller | – | STM32F334R8T6 |
| Primary-side transistor drivers | – | ADUM3221 |
| Secondary-side transistor drivers | – | ACPL-P346 |

The experimental waveforms for the APRC topology at $V_{in}$ = 24 V are presented in Figs. 4 and 5. As shown in Fig. 4, top switch S1 is turned off when the resonant current is flowing through its body diode, resulting in ZCS. Bottom switch S2 is turned off when its current is taken over by S4, which also results in ZCS. All the primary switches turn on with reduced d$i$/d$t$ and, as a result, the turn-on losses diminish. The input current waveform in Fig. 5 shows that the converter continues to be in the shoot-through state during the resonant period, while the transformer secondary winding changes polarity.

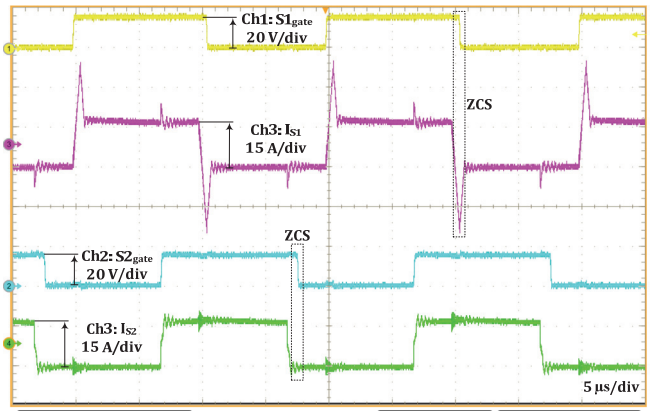


Fig. 6. Experimental waveforms of an ASMC converter: Ch1 – S1 gate voltage, Ch2 – S2 gate voltage, Ch3 – S1 current and Ch4 – S2 current.

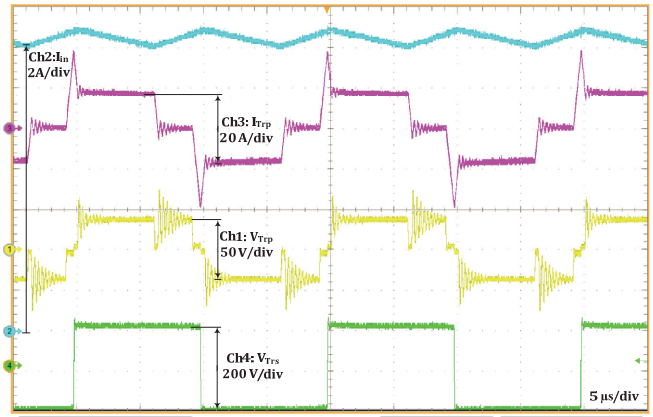


Fig. 7. Experimental waveforms of an ASMC converter: Ch1 – $V_{Trp}$, Ch2 – $I_{in}$, Ch3 – $I_{Trp}$ and Ch4 – $V_{Trs}$.

The measurement results of ASMC at $V_{in}$ = 24 V are shown in Figs. 6 and 7. During the experiments, the converter was operating with a very small value of $C_{eq}$ and, as a result, the $t_4$–$t_5$ interval is minor. Similar to the APRC topology, the top transistors turn off when their body diode conducts, while the bottom ones – after the current drops to zero, resulting in ZCS for all the primary semiconductors. From Fig. 7 it can be observed that the transformer secondary voltage changes polarity when its current is at the peak value and, since $C_{eq}$ could be small for this converter, the process takes significantly less time. During the laboratory experiments, the power stage of ARPC reached an efficiency of 96.4 % and that of ASMC – 96.6 % at an input voltage of 30 V.

The experimental results are in agreement with theoretical estimations for both topologies and therefore it can be concluded that the claims presented in the previous sections have been confirmed.

## IV. Conclusion

This paper introduced two isolated soft-switching asymmetric current-fed DC-DC converters with a passive rectifier and an active one. The proposed topologies can be applied in systems where a high gain and/or galvanic isolation are required, such as fuel cells, batteries, DC microgrids and other applications. The converters have two reverse-blocking devices and two reverse-conducting ones at the primary side and utilize phase-shift control with a constant switching frequency. Their main aim is to reduce the problem of high circulating energy encountered in existing symmetric topologies and the high conduction losses present in topologies with phase-shift control.

The experimental results showed a peak power stage efficiency of 96.4 % and 96.6 % for the ARPC and ASMC topologies, respectively. That proves that the topologies proposed allow achieving a comparable level of efficiency – while having a lower switch count than other existing topologies with a phase-shift control algorithm and lower current stress than the topologies with a symmetrical modulation control algorithm.

Future research will focus on the detailed analysis of the presented topologies and their comparison with other existing solutions, designed with the same constraints and requirements.

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