sciendo RIGA TECHNICAL UNIVERSITY *Electrical, Control and Communication Engineering*

ISSN 2255-9159 (online)
ISSN 2255-9140 (print)
2019, vol. 15, no. 2, pp. 113–118
doi: 10.2478/ecce-2019-0015
https://content.sciendo.com

A 79 dBΩ 1.2 GHz Low-Noise Single-Ended CMOS Transimpedance Amplifier for High-Performance OTDR Applications

Agata Romanova* (*PhD Student, Department of Computer Science and Communication Technologies, Vilnius Gediminas Technical University, Vilnius, Lithuania*),
Vaidotas Barzdenas (*Prof., Micro and Nanoelectronics System Design and Research Laboratory, Vilnius Gediminas Technical University, Vilnius, Lithuania*)

***Abstract* – The work reports on the design and performance of a low-noise low-cost CMOS transimpedance amplifier (TIA). The proposed circuit shall be employed in optical time-domain reflectometers and is implemented using an affordable 0.18 µm 1.8 V CMOS process. The approach preserves the benefits of a classical feedback structure while addressing the noise problem of conventional feed-forward and resistive feedback architectures via the usage of noise-efficient capacitive feedback. Circuit-level modifications are proposed to mitigate the voltage headroom and DC current issues. The suggested design achieves a total gain of 82 dBΩ (79 dBΩ after the output buffer) within the bandwidth of 1.2 GHz while operating with a total input capacitance of 0.7 pF. The simulated average input-referred noise current density is below 1.8 pA/sqrt(Hz) with the power consumption of the complete amplifier including the output buffer being 21 mW.**

***Keywords* – Analog integrated circuits; broadband amplifiers; CMOS integrated circuits; optical time-domain reflectometry; transimpedance amplifier.**

I. Introduction

The constantly increasing requirements for available data rates and even larger capacities in communication systems have led to wide adoption of optical data transmission systems. As a result, the intensive deployment of the required infrastructure boosted interest in the related instrumentation and maintenance equipment for network monitoring and repairs. Here the tools based on Optical Time-Domain Reflectometry (OTDR) [1] are one of the typical instruments for characterization of the optical fiber links. The precise location and the nature of the problem in the fiber can be resolved from an accurate time-domain measurement of the reflected optical pulse. The technique works, first by injecting a series of relatively narrow optical pulses to the fiber and then monitoring the properties of the reflected signals caused by the Rayleigh Backscattering or Fresnel reflections. The analysis of the reflected signal allows not only estimation the general dependency of the fibre loss characteristics on the length of the fiber, but also permits detection of major faults and identification of their types by observing the properties of the reflected signals (timing, amplitude, etc.) at the input of the very same fiber.

Like in the case of a classical optical receiver, the OTDR equipment contains a conventional Transimpedance Amplifier (TIA) as an integral part of the front-end. The block shall be considered as one of the most important parts of the instrument with its performance often limiting the overall sensitivity of the measurement device. Although the present research considers the seemingly typical problem of developing a Complementary Metal-Oxide-Semiconductor (CMOS) TIA, a different set of the requirements shall be considered when compared to the design of a CMOS TIA for conventional data transmission applications in optical networks. Note that those have been historically developed with the major emphasis on bandwidth and gain with often reduced importance for noise, ripple in the passband and the linearity. However, the latter shall be considered as important constraints for OTDR applications and will have a significant impact on the selection of the design for the target application.

The TIA is essentially a current measurement device which is responsible for conversion of the weak input current (e.g. from the photodiode or any other sensor with current output) to the output voltage of sufficient amplitude. When discussing TIA, one typically recalls the resistive shunt-feedback (SFB) resistive approach [2] which is almost universally accepted as a reference TIA design. This shall come as no surprise as this approach, although known for a longer time, provides a fair balance for the most important parameters of the TIA including noise, bandwidth, power consumption and the gain. Unfortunately, some of the requirements, which are specific to OTDR applications, make a design of the corresponding TIA a challenging task when compared to basic CMOS TIA architectures typically employed in optical networks. First, recent design approaches based on high-speed feed-forward architectures are likely to be eliminated due to the OTDR requirement for a relatively low noise level, especially when one considers instruments beyond those for trivial discontinuity detection in the fiber. The same requirement may also eliminate the topologies based on resistive feedback due to noise issues as discussed elsewhere [2]. The requirement of the OTDR instrument for the ripple in the pass band (<0.5 dB) may also question the methods which rely on inductive peaking for

* Corresponding author.
E-mail: agata.romanova@vgtu.lt

bandwidth extension or, at least make them less attractive when compared to inductor-less designs. Note, however, that the inductor-based bandwidth extension techniques may appear even unnecessary as the performance of modern commercially available CMOS is sufficient for the envisioned OTDR equipment with time resolution performance equivalent to bandwidth requirements up to 1 GHz. The constraints for the OTDR instrument to employ off-chip photodetectors result in requirements for the amplifier to support large input parasitic capacitance $C_{\mathrm{IN}} > 0.7$ pF. This includes not only the photodiode capacitance itself, but also the rest of the input parasitics, e.g., those of bond pads, ESD circuits, etc. Here a relatively large input capacitance can lead to inherent bandwidth limitations due to the dominant pole in the TIA transfer function and may result in significant bandwidth constraints if the issue is left unaddressed [4]. Finally, a relatively large gain of 10 kΩ must be delivered with 1 GHz bandwidth, while the noise density shall be less than 5 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ within the target bandwidth.

Historically, the technologies such as GaAs, HEMT, HBT and SiGe BiCMOS have been employed for the production of higher performance TIAs [5]. Although these technologies have performance advantages over low-cost deep submicron CMOS in terms of the noise, gain and bandwidth, the latter was chosen for the presented design due to costs and unquestionable potential for higher integration. Significant performance enhancement functionality such as complex biasing circuits and advanced ESD design procedures can be added at almost no costs in conventional CMOS. Although CMOS technology is an excellent choice for cost-saving purposes, some technological challenges shall be addressed while realizing an envisioned TIA in CMOS. The issues include noise performance, limitations in supply voltage and severe parasitic capacitances [6].

A classical SFB TIA with its feedback topology is shown in Fig. 1 [7]. This approach results not only in low input impedance as required for the current input block, but also ensures relatively low output impedance as required for voltage output amplifiers [8]. Although extensive modifications on this classical architecture have been reported such as the addition of the appropriately sized feedback capacitor for the improved flatness of the frequency response, the topology has a number of inherent drawbacks which make it hard to implement a truly high-performance front-end. The limiting factors include the sensitivity to the parasitic capacitance and the stability issues which can make it impossible to obtain the required set of the major performance numbers for the given large input capacitance. These known challenges resulted in the development of alternative approaches including so-called common-gate (CG) and regulated cascade (RGC) TIAs. Even though the designs were able to address some of the problems typical for SFB TIA, they have introduced the performance issues on their own. Among those, poor noise performance of classical feed-forward designs makes them unsuitable for higher performance OTDR applications even though the designs may demonstrate excellent gain and bandwidth performance.

Although some works have demonstrated promising results while using monolithic inductors in CMOS [3], we will pursue for an inductor-less approach due to several reasons. Even though the inductors in CMOS have been intensively used for more than 20 years, the design relying on their usage may still lead to an increase of the final chip size. The design may also result in increased substrate coupling and lead to higher cross-talks when compared to designs without inductors. Finally, it may be non-trivial to preserve the required inductive characteristics of the components over the complete intended bandwidth as have been discussed in [9].

The amplifiers as employed in commercial OTDR instruments have been traditionally implemented using discrete components. Due to the small production volume of the instruments, the strategy resulted in TIA bandwidth close to 50–70 MHz and caused significant performance limitation [1]. Here an integrated CMOS TIA solution will not only deliver an improved performance due to lower parasitics and, thus, increased bandwidth, but will also lead to higher flexibility and fine-tuning of the design – something, which is not easily possible within an approach based solely on discrete components. A unique work reported on TIA design for OTDR application is [1], where a variable-gain fully differential design was proposed using a conventional SFB TIA topology. The feedback resistors connected in series were employed to implement the variable gain, while as few as five resistor pairs were shown to be enough to cover the desired range of gain and bandwidth combinations. The authors did not consider possible design optimizations towards lower noise figures and exact noise level of the solution has not been provided. Several works also reported systems with complete OTDR functionality on a single chip [10], [5]. However, either no details on the TIA structure have been included [10] or trivial designs such as SFB TIA with a feedback capacitor have been used [5], [11].

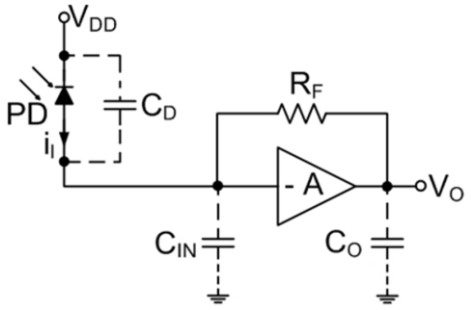

Fig. 1. Basic configuration of resistive SFB TIA.

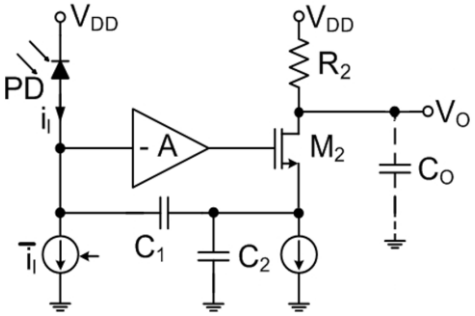

Fig. 2. Concept of capacitive feedback TIA.

II. Circuit Design

As the noise current of the feedback resistor R_F is directly added to the input noise current in SFB TIA, the noise performance of this classical design cannot be easily addressed without sacrificing other key performance indicators. Here one may think on improving the noise figures by replacing the noisy R_F with a noise-free element such as a capacitor. However, a trivial replacement of the resistor with capacitor, while eliminating the noise caused by the feedback element, will add a phase shift of 90° which needs to be corrected afterwards. Yet another approach with noiseless feedback network is shown in Fig. 2 and was first demonstrated by Razavi in [12]. The solution eliminates the issues caused by the classical feedback resistor while preserving the advantageous feedback structure of the topology without a necessity for subsequent phase correction stages. The proposed design is based on two capacitances C_1 and C_2, where the former senses the voltage across the latter and the proportional current is returned to the input. For a typically high core gain $A \gg 1$, the current gain can be approximated as:

$$\frac{I_{\text{out}}}{I_{\text{in}}} \approx 1 + \frac{C_2}{C_1}. \tag{1}$$

The expression suggests that the circuit is a current amplifier and with the resistor R_2 connected to the transistor M_2 characterised by the transconductance $g_{\text{m},M2}$, the low-frequency gain becomes:

$$R_{\text{T}} = \left(1 + \frac{C_2}{C_1}\right) R_2, \tag{2}$$

while the bandwidth is shown [8] to be:

$$BW_{-3\text{dB}} = \frac{(1+A) g_{\text{m},M2}}{2\pi C_2}. \tag{3}$$

If the input stage is implemented as a common-source (CS) with resistor R_1 and transistor M_1, the calculation for noise will deliver [8]:

$$\overline{\iota_{n,\text{TIA}}^2} = \frac{4kT\gamma}{g_{\text{m},M2}} \left[\left(\frac{C_2}{1 + C_2/C_1} + C_{\text{IN}} \right) s \right]^2, \tag{4}$$

where C_{IN} is the total input capacitance. The characteristic is valid for higher values of resistor R_1 which is often true as it is typically set high for improved noise performance while considering the limitations of the voltage headroom. In the expression above γ is the noise excess factor, T is the absolute temperature and k is the Boltzmann's constant. The expression for the DC gain as shown above, although being valid under perfect circumstances (see discussion in [8], [12]), for realistic amplifier configuration shall be replaced with:

$$R_{\text{T,DC}} = \frac{R_2 \left(C_2 + R_1 g_{\text{m},1} (C_1 + C_2) \right)}{C_2 R_1 g_{\text{m},1} + C_2 + C_{\text{IN}}}, \tag{5}$$

with the total transfer function in s domain:

$$R_{\text{T}} = R_{\text{T,DC}} \frac{1}{\left(1 + \frac{s(C_1 C_2 + C_1 C_{\text{IN}} + C_2 C_{\text{IN}})}{g_{\text{m},2}\left(C_2 R_1 g_{\text{m},1} + C_2 + C_{\text{IN}} \right)} \right)}. \tag{6}$$

The relationship above assumes the performance of the core voltage amplifier (CS in our case) being unconstrained within the bandwidth of interest, although it is not the case for an intended 1 GHz OTDR application. Consequently, the bandwidth as estimated from the expression above may be strongly overestimated when compared to a behaviour of a real circuit with given power supply constraints.

For more realistic modelling it may be useful to replace the gain of the core voltage amplifier with a first-order low-pass approximation in the following form:

$$G = R_1 g_{\text{m},1} \rightarrow g_{\text{m},1} \frac{R_1}{1 + \frac{s}{\omega_{\text{c}}}}, \tag{7}$$

where ω_c is the cut-off frequency of the corresponding low-pass approximation. The correction from above does not affect the generic model of the DC gain, which for low frequencies remains $R_1 g_{\text{m},1}$. A trivial algebraic manipulation on the expressions above leads to the following complete transfer function of the capacitive feedback TIA with a first-order approximation for core CS amplifier:

$$R_{\text{T}} = \frac{R_2 g_{\text{m},2} \left(C_2(\omega_c + s) + R_1 \omega_{\text{c}} g_{\text{m},1} (C_1 + C_2) \right)}{A_1 + A_2}, \tag{8}$$

with denominator coefficients correspondingly: $A_1 = g_{m,2} \left(C_2 R_1 \omega_c g_{\text{m},1} + (C_2 + C_{\text{IN}})(\omega_{\text{c}} + s) \right)$, and $A_2 = s(\omega_{\text{c}} + s)(C_1 C_2 + C_1 C_{\text{IN}} + C_2 C_{\text{IN}})$.

The presented relationship ensures a consistent estimation of the TIA bandwidth when compared to the simplified modelling as demonstrated in [8], [12]. Moreover, the formulation from above serves as a basis for an improved design methodology where, e.g., the circuit parameters C_1 or R_1 can be computed from the circuit gain and bandwidth requirements. A sole remark is that for the new expressions above to hold an operating point for M_1 shall be established. For the given supply voltage this may be achieved by controlling the current source (see Fig. 3), which shall be adjusted for a particular R_1. This fact is also extremely important for the planned variable-gain TIA where the change of C_1 and/or R_1 shall be accompanied with a proper adjustment of the current source formed by M_3.

The circuit from above has several advantages when compared to well-established TIA designs [12]. First, the gain is defined solely by C_1 and C_2 and introduces no noise to the system. The capacitance at the input node does not degrade the stability of the circuit and only lowers the DC loop gain. Finally, the first stage of the amplifier contributes less noise when compared to SFB TIA. The overall gain, at least in theory, is defined by the ratio of C_1 and C_2 and, thus, results in the

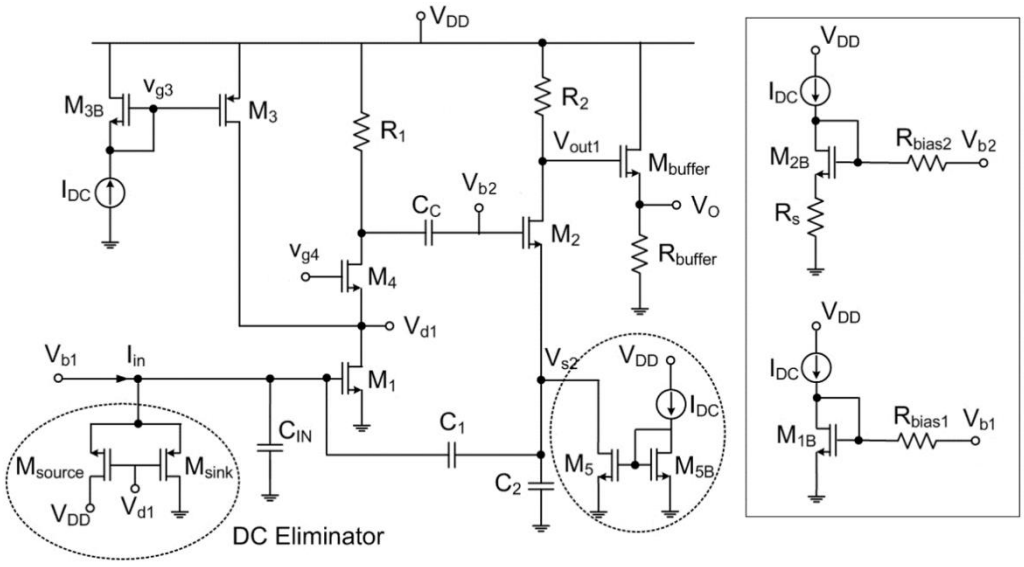

Fig. 3. The implementation of the amplifier circuit with associated bias circuits and the output buffer.

design which is less sensitive to the variations in the production process when compared to the approaches which rely on the absolute value of the resistance in the feedback loop. Note that for the linear operation the bias current (the left-most current source) shall be larger than $I_{\mathrm{in,max}}(1 + C_1/C_2)$ and, therefore, the noise contribution of R_2 and of that current source may be still of relevancy.

Although the noise of M_2 and that of the current source are also important, the noise impact of M_2 can be made negligible following necessary design guidelines. The output stage of the proposed amplifier can be considered as a voltage source in series with a gate. This divides the noise contribution by the gain A resembling the generic behaviour of the CG TIAs [2]. The approach has also clear advantages when compared to feed-forward designs as the noise current of R_2 and that of the current source is divided by $(1 + C_2/C_1)$. Moreover, although in popular feed-forward common-gate TIA the gain is $R_\mathrm{T} = R_2$, here it is also amplified by the same factor $(1 + C_2/C_1)$.

Fig. 3 demonstrates the detailed structure of the suggested TIA including two biasing circuits and the output buffer. A single-stage common-source (CS) voltage amplifier is used as a core amplifier. Although more advanced designs are clearly possible, the strict noise requirements imposed by OTDR favour simpler voltage amplifies with the minimum number of active components [9]. Thus, a basic single-stage CS design is adopted here under the assumption that enough gain may be achieved with the provided configuration. The Miller effect of M_1 is addressed by introducing an additional NMOS (M_4) on top of M_1. The former is biased with V_{g4} to 1.4 V and serves a purpose to reduce the overall input capacitance and to improve the combined noise performance of the design.

As the accuracy of the feedback is strongly dependent on the gain of the core amplifier, one may try to increase R_1. However, a straightforward approach is likely to be limited due to the voltage headroom problem for the given 1.8 V CMOS. Thus, to increase R_1 while avoiding a decrease in the current density for M_1, an additional PMOS M_3 is introduced in parallel with the resistive load. The new combined load will control the current which is fed through M_1. Here the increase in the load resistance will reduce its noise current, while the noise current of the newly added M_3 is minimized via dedicated bias V_{g3}. The final circuit is configured with 80 % if the current provided by M_3 and the rest passing through the resistive load. The modification minimizes the noise caused by the resistive load, while a sufficient gain may be still obtained from this simple CS structure of the core amplifier.

The operating principles of the OTDR instrument require the lower cut-off frequency of the front-end amplifier to be 100 kHz. A classical design approach for biasing circuits, as shown in Fig. 3, may require significant series resistors to be connected to the gates of M_1 and M_2 while minimizing parasitic capacitances. Although an interesting solution had been proposed in [8], where a combination of 3 NMOS transistors was employed to construct the bias circuit, the approach is not feasible for the presented 1.8 V design due to voltage headroom problems (the authors in [8] employed a 2.2 V power supply). In the proposed design we still use an area-inefficient approaches for both biasing circuits V_{b1} and V_{b2}, while only the latter is of a major issue with the bias resistor taking around 70 % of the total area. Note that additionally a resistor R_s is introduced to the bias circuit for M_2 in order to improve the voltage control of the transistor source.

A typical problem with this type of circuits is the DC dark current which may cause the circuit saturation or even result in instability. Although often the off-chip solutions are adopted to mitigate the problem, the proposed design follows implementation of [8], [12] with two transistors forming DC eliminator block as shown in Fig. 3. Both sink and source transistors shall have a minimum width if design with minimum noise current is necessary. Finally, a specially designed current mirror is used for V_{s2} with a classical output buffer implemented for output load matching (50 Ω).

III. Results

The circuit as discussed above was designed, optimised and implemented using TSMC 0.18 μm process. The area of the

complete circuit fits 150 μm × 200 μm as can be seen in Fig. 4. The post-layout simulation results for the transimpedance gain and the input-referred noise currents are shown in Fig. 5 and Fig. 6 correspondingly.

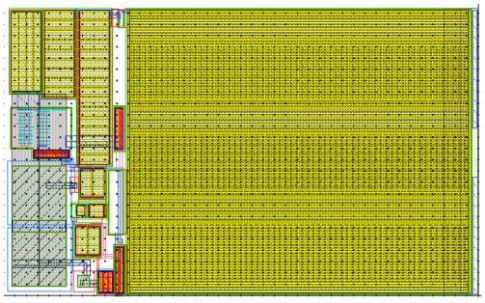

Fig. 4. Layout of the implemented TIA.

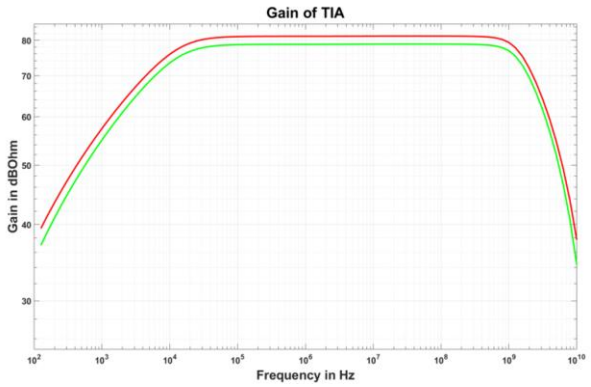

Fig. 5. Simulation results for the transimpedance gain before (red line) and after the output buffer (green line).

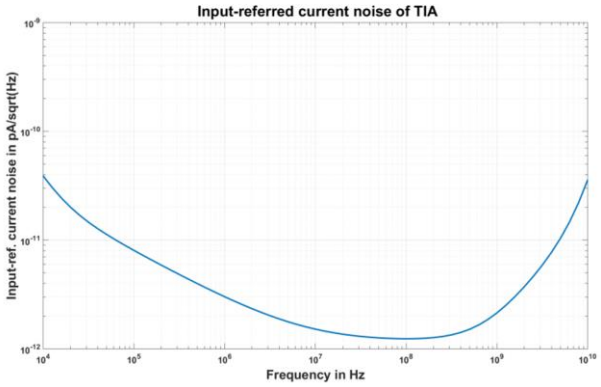

Fig. 6. Simulation results for input-referred current noise.

The design results in 82 dBΩ transimpedance gain (2.5 dBΩ drop at the output buffer) over the bandwidth of 1.2 GHz. The ripple within the bandwidth is insignificant and is below 0.5 dBΩ as imposed by OTDR. The input-referred current noise is below 1.8 pA/$\sqrt{\text{Hz}}$ and ensures sufficient margin for future circuit modifications such as an extension of the proposed single-ended approach to differential design.

The simulation results are given for C_{IN} = 0.7 pF with the main circuit parameters as follows: C_1 = 2.2 pF; R_1 = 300 Ω; and R_2 = 450 Ω. A classical source follower is added for 50 Ω output matching and C_2 is taken five times the minimum capacitance. The current through M_1 is approximately 10 mA with around 8 mA passing through M_3 and the rest 2 mA through R_1. The current through M_2 is set to only 600 μA. As the output buffer requires also 600 μA, the total current of little more than 11 mA is drawn by a complete single-ended TIA configuration. The complete design including the output buffer shows the total power consumption of 21 mW while running at 1.8 V supply. Similarly, to the case of noise performance, the non-differential design shown in this research ensures sufficient margin for differential extension (OTDR differential TIA specification opts for < 50 mW power consumption).

IV. Discussion

A tremendous growth of the market for optical communication systems, when compared to niche OTDR, caused a large number of CMOS TIA designs proposed in the last decades. Although the TIA design targeting OTDR must obey a set of application-specific constraints such as high linearity and low-noise, some of the designs originally suggested for optical data transmission are, at least in principle, directly applicable for OTDR TIAs with only modest modifications.

In order to evaluate the performance of the proposed design with respect to other CMOS TIAs, the following Figure-Of-Merit (FOM) is proposed to combine all the key performance indicators within a single number:

$$FOM = \frac{\sqrt{BW[\text{GHz}]}R_{\text{T}}[\Omega]C_{\text{IN}}[\text{pF}]}{Noise\left[\text{pA}/\sqrt{\text{Hz}}\right]P[\text{mW}]}. \quad (9)$$

In the expression above BW stands for the bandwidth of the TIA, C_{IN} is the total input parasitic capacitance, P is the power consumption and *Noise* is the density of the input-referred noise current. In terms of the proposed FOM, the circuit achieves the performance of approximately 180 units with only several recent works [8], [13] showing better numbers. However, the work [8] reports no exact value of the C_{IN} used (we use a default value of 0.5 pF for FOM calculation), whereas the design [13] used a far more advanced 40 nm CMOS. Note that not all promising designs have been described with enough details for the FOM to be calculated. Often, the authors omit some of the details and do not specify explicitly whether the power consumption of the core TIA or that of a complete solution, including the output buffer and auxiliary circuits, is provided. Similarly, often information is missing on the exact value of the input capacitance or the photodiode capacitance is not distinguished from the rest of the input parasitics. The proposed FOM does not include a penalty term due other OTDR-relevant characteristic such as the nonlinearity of the ripple in the passband as these numbers are often not available in published works. Some promising designs have been demonstrated without explicit requirements on the flatness of the response and ultimate performance of these approaches under OTDR constraints may be a subject of future research. Recall that in the reference capacitive feedback TIA the feedback gain is determined by the ratio of capacitors C_1 and C_2 and this fact was used in [8], [12] to claim for an advantage of the design as

an area-efficient implementation with poly capacitors could be used for a reduced vulnerability to process variations. The results above show that original Expression (2) may be overoptimistic as the definition for the gain is more intricate under-voltage headroom constraints and this promising feature of the topology may not be fully realisable. Comparative analysis also reveals that the proposed design does not lead to extremely low power when compared to some modern feed-forward TIAs.

Despite many works on the design of TIA in CMOS, only a few discuss (see [13], [14]) an impact of process variation on the circuit performance and a comparative study of the proposed TIA with respect to classical TIA topologies may be an interesting research topic.

V. Conclusion

The design of a low-noise CMOS transimpedance amplifier for OTDR applications was proposed in the paper. The inductor-less circuit was realized using a 0.18 µm 1.8 V CMOS process and is based on a capacitive feedback architecture. The post-layout simulation demonstrated the circuit gain of 82 dBΩ (79 dBΩ with output buffer) with the bandwidth reaching 1.2 GHz at 0.7 pF total input capacitance. The design shows the average input-referred noise current below 1.8 $pA/\sqrt{Hz}$ with total power consumption around 21 mW. The developed solution eliminates the major drawbacks of classical resistive feedback or feed-forward TIA designs and results in a better trade-off for all the major circuit performance measures while preserving the fundamental advantage of the feedback structure. A more accurate design procedure is suggested while considering the limited bandwidth of the core voltage amplifier. Future research is planned on optimization of the chip area, improvement of the bias circuits and a variable-gain version of the circuit.

References

[1] J. Charlamov and R. Navickas, "Design of CMOS Differential Transimpedance Amplifier," *Elektronika ir Elektrotechnika*, vol. 21, no. 1, pp. 38–41, 2015. https://doi.org/10.5755/j01.eee.21.1.4548

[2] E. Sackinger, *Analysis and Design of Transimpedance Amplifiers for Optical Receivers*. John Wiley & Sons, 2018. https://doi.org/10.1002/9781119264422

[3] S. S. Mohan et al, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 346–355, March 2000. https://doi.org/10.1109/4.826816

[4] O. Momeni, H. Hashemi, and E. Afshari, "A 10-Gb/s Inductorless Transimpedance Amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 12, pp. 926–930, Dec. 2010. https://doi.org/10.1109/TCSII.2010.2087971

[5] J. H. Yeom, K. Park, J. Choi, M. Song, and S. Y. Kim, "Low-cost and high-integration optical time domain reflectometer using CMOS technology," in *2019 15th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, July 2019, pp. 145–148. https://doi.org/10.1109/PRIME.2019.8787845

[6] J. D. Jin and S. S. H. Hsu, "40-Gb/s Transimpedance Amplifier in 0.18-µm CMOS Technology," in *2006 Proceedings of the 32nd European Solid-State Circuits Conference*, Sept 2006, pp. 520–523. https://doi.org/10.1109/ESSCIR.2006.307504

[7] H. Escid, S. Salhi, and A. Slimane, "Bandwidth enhancement for 0.18-µm CMOS transimpedance amplifier circuit," in *2013 25th International Conference on Microelectronics (ICM)*, Dec 2013, pp. 1–4. https://doi.org/10.1109/ICM.2013.6734945

[8] S. Shahdoost, A. Medi, and N. Saniei, "Design of low-noise transimpedance amplifiers with capacitive feedback," *Analog Integrated Circuits and Signal Processing*, vol. 86, no. 2, pp. 233–240, 2016. https://doi.org/10.1007/s10470-015-0669-x

[9] J. D. Jin and S. S. H. Hsu, "A 40-Gb/s Transimpedance Amplifier in 0.18-µm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1449–1457, June 2008. https://doi.org/10.1109/JSSC.2008.922735

[10] C. Kuznia, J. Ahadian, D. Pommer, R. Hagan, P. Bachta, M. Wong, K. Kusumoto, S. Skendzic, C. Tabbert, and M. W. Beranek, "Novel high-resolution OTDR technology for multi-Gbps transceivers," in *OFC Conference*, March 2014, W1F.2, pp. 1–3. https://doi.org/10.1364/OFC.2014.W1F.2

[11] A. Romanova and V. Barzdenas, "A review of modern CMOS transimpedance amplifiers for OTDR applications", *Electronics 2019*, 8(10), 1073. https://doi.org/10.3390/electronics8101073

[12] B. Razavi, "A 622 Mb/s 4.5 pA//spl radic/Hz CMOS transimpedance amplifier for optical receiver front-end," in *2000 IEEE International Solid-State Circuits Conference*. Digest of Technical Papers (Cat. No.00CH37056), Feb. 2000, pp. 162–163. https://doi.org/10.1109/isscc.2000.839732

[13] M. Atef and H. Zimmermann, "2.5Gbit/s transimpedance amplifier using noise cancelling for optical receivers," in *2012 IEEE International Symposium on Circuits and Systems*, May 2012, pp. 1740–1743. https://doi.org/10.1109/ISCAS.2012.6271599

[14] M. Atef and D. Abd-Elrahman, "2.5 Gbit/s compact transimpedance amplifier using active inductor in 130 nm CMOS technology," *2014 Proceedings of the 21st International Conference Mixed Design of Integrated Circuits and Systems (MIXDES)*, 2014, pp. 103–107. https://doi.org/10.1109/MIXDES.2014.6872165

Agata Romanova was born in Vilnius, Lithuania, in 1988. She received the B.S. degree in electronic and electrical engineering from Vilnius Gediminas Technical University, Lithuania, in 2010 and M.S. degree in microsystems engineering from Hochschule Furtwangen University, Germany, in 2012. Since 2017 she has been working towards her PhD degree at the Department of Computer Science and Communication Technologies, Vilnius Gediminas Technical University.

Between 2012 and 2016, the author worked at the Leibniz Institute for High-Performance Microelectronics (IHP), Frankfurt (Oder), Germany, where she was involved in design and characterisation of semiconductor circuits. Her research interests include design and layout of analogue and mixed-signal integrated circuits.

Address: Department of Computer Science and Communication Technologies, Vilnius Gediminas Technical University, Naugarduko Str. 41, Room 435, LT-03227, Vilnius, Lithuania.

E-mail: agata.romanova@vgtu.lt

Vaidotas Barzdenas was born in Vilnius, Lithuania, in 1980. He received the B.S., M.S., and Ph.D. degrees in electronic and electrical engineering from Vilnius Gediminas Technical University (Lithuania) in 2002, 2004 and 2008, respectively. He is currently a Professor at the Department of Computer Science and Communications Technologies and a Senior Research Fellow at the Micro- and Nanoelectronics Systems Design and Research Laboratory, Vilnius Gediminas Technical University.

His current research interest includes the novel micro- and nanoelectronics technologies, RF, digital, analogue and mixed-signal integrated circuit design and layout, and their optimisation algorithms, synthesis and analysis methods. His educational research interests include active learning methodologies, education media and technologies.

Address: Micro and Nanoelectronics System Design and Research Laboratory, Vilnius Gediminas Technical University, Saulėtekio Ave. 3-B118, Room LT-10257, Vilnius, Lithuania.

E-mail: vaidotas.barzdenas@vgtu.lt

ORCID iD: https://orcid.org/0000-0002-8988-875X