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A New Quasi Open Loop Synchronization Technique for Grid-Connected Applications

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***Abstract* – This paper presents an effective quasi open-loop (Q-OLS) synchronization technique for grid-connected power converters that is organized in two different blocks. The first block is a new flexible technique for extracting the positive and negative sequence voltage under unbalanced and distorted conditions. It is a decoupled double self-tuning filter (DD-STF) or multiple self-tuning filters (M-STF) according to the conditions. The main advantages of this technique are its simple structure and the fact of being able to work under highly distorted conditions. Each harmonic is separately treated and this allows for selective compensation in active filter applications. The second block is the frequency detector; we propose a neural approach based on an ADALINE for online adaptation of the cut-off frequency of the DD-STF and M-STF considering a possible variation in the main frequency. The main advantage of this method is its immunity to the voltage signal amplitude and phase. In order to improve the performance of the frequency estimation under distorted source voltage, a pre-filtering stage is introduced. Experimental tests validate the proposed method and illustrate all its interesting features. Results show high performance and robustness of the method under low voltage ride through.**

***Keywords* – Adaptive linear neuron (ADALINE); Distributed energy sources (DES); Low voltage ride through operation (LVRT); Open loop synchronization (OLS); Self-tuning filter (STF).**

I. Introduction

In recent years, the increased energy demand and technological advances in semiconductor technology and signal processing have made power converters more efficient and less expensive, and are now widely used for interfacing renewable energy such as wind turbines and photovoltaic for the connection to the main grid and/or local loads [1]–[8]. These energies have high levels of penetration and can affect power quality. Prior to 2003, the utility grid did not contain any requirements for the LVRT or fault ride-through (FRT) of wind systems (WS). Many countries have recently updated the grid codes. Among these, the German grid code implemented by Eon-Netz in 2003 and 2011 requires that the (WS) must be connected by providing reactive power to the grid, it is when the voltage drop is below the guideline of the grid code the (WS) is disconnected. Besides, from January 2011 the FRT of photovoltaic (PV) installations had full participation in the dynamic support of grid in faulty conditions: to stay connected and provide voltage support by injecting a reactive current into the grid. These requirements have made the synchronization task more challenging than before [7], [8].

Synchronization is a very important unit in the control of power converters; it is a coordination procedure of the converter and the main grid to have an efficient operation in parallel. Synchronization techniques can be classified into open loops and closed-loops [9]–[25]. In the closed-loops, there are two different categories: the phase-locked loops (PLL) and the frequency locked loops (FLLs).

The synchronous reference frame with PLL (SRF-PLL) is the most widely used synchronization in power converter. A PLL is a nonlinear feedback control system implemented in the synchronous coordinate and synchronizing its output signal with the fundamental component of the grid voltage, which is its input signal [13]. From the phase estimation point of view, the PLL with PI LF is a control system of type 2 because the transfer function of its linearized model has two poles at the origin [10]. Therefore, it can follow a phase jump that corresponds to a frequency jump with a zero error in steady-state and it is not the case in frequency ramps. Besides, the PLL loop gain depends on the amplitude of the grid voltage. Any variation in this amplitude modifies the gain of the PLL loop, thus, its dynamics and stability characteristics. This situation may happen under voltage sags and faults. To be more exact, it suffers from poor disturbance rejection under highly unbalancing and distorted conditions [10]. Another disadvantage of conventional PLL is the vulnerability to the presence of the dc offset in its input, which can come from grid faults and dc injection by distributed generation systems [14], [15]. The unit vector of the PLL (sine and cosine functions) in this case contains a DC component; this vector is used for reference current generation in the grid-connected converter, which leads to injecting a DC current by the converter to the grid. Furthermore, the standards IEC61727 and IEEE 1547-

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2003 have limited injecting the DC current, this limit being respectively 1 % and 0.5 % of the nominal current of the converter. On the other hand, even a narrow bandwidth PLL cannot effectively mitigate the previously cited issues. Also reducing the PLL bandwidth significantly degrades its dynamic response. These disadvantages of PLL have been the main motivation for recent efforts to design more efficient PLLs. Roughly speaking, these efforts often result in the following: 1) it is not possible to attain a response time lower than 2 cycles of the nominal frequency [16]; 2) it is less attractive to overcome the dc offset problem [14], [15]; 3) there is high computational burden; 4) there is implementation complexity; 5) there is inefficiency under high-frequency drift and highly distorted source voltage. This fact is discussed in more detail in [10]. Other approaches increase the PLL type by one (type 3) [17] (three open-loop poles at the open-loop phase transfer function of the PLL) to enhance the dynamic performance and the tracking capability in frequency ramps (zero steady-state phase error). There are several methods to implement the type 3 PLLs [10], the simple is to replace the PI LF by the controller of the reference [17], using this controller; however, the result in a negative gain margin, which can cause instability in case of the reduced loop gain. On the contrary, a type 1 PLL is unconditionally stable but unfortunately cannot achieve zero steady-state error during frequency step change [18].

Recently, FLL emerges as another closed-loop approach [19]–[25]. But unlike PLL, the control system locks the frequency instead of the phase to obtain the performance of type 2 PLL using type 1 control system. FLLs are implemented in the stationary reference frame using generalized integrators, making it more difficult to design additional filters to be incorporated into their structures. Thus, stability in this condition requires deep analysis, often complicated by the non-linearity caused by FLL. These facts generate the search for new contributions that serve to facilitate the FLL modelling procedure and improve their filtering. Reference [12] provides an overview of the latest developments in FLLs and also contributes to the modelling of their small signal and improves their filtering capacity through the concept of the loop filter. In this reference, two examples were examined: the αβ delayed signal cancelation operator chain (DSC) and a first-order complex band pass filter (CBF) corresponding respectively to loop filter FLLs and it has been shown that the loop filter improves the disturbance rejection capability, but unfortunately reduces its stability margin. On the other hand, it has also been shown that FLLs are mathematically equivalent to PLLs. This means that FLLs and PLLs are virtually the same control systems as those implemented in different reference frames. In addition, higher penetration of renewable energy resources or the weak grid condition, the dynamic interaction between a PLL or FLL and the converter make the PLL or FLL and, therefore, the converter unstable [27] if the conventional vector current control is applied. The PLL introduces negative incremental resistance at low frequencies and [28] has shown the frequency coupling dynamics of the converter introduced by the PLL. To improve the stability of the converter, low bandwidth is adopted. Using this technique, the dynamic response is significantly reduced and keeping the converter stable under a grid impedance of 1.3 pu [29]–[32] is difficult under a weak grid condition. Consequently, a PLL (or FLL) is omitted in such a condition to guarantee the stable operation of the converter [33].

Open loop synchronization (OLS) is a newly emerging technique that omits the feedback signal in its structure, which results in unconditional stability [9], [11]. This is probably the main advantage of an OLS technique over PLL and FLL. In addition, simplicity and fast dynamic response are other characteristics of the OLS techniques. Despite these advantages, they suffer from a serious drawback: they may not operate efficiently under off-nominal frequencies. To tackle this issue, the widely used solution is including a parallel frequency detector to make them adaptive [34]–[36]. This technique depends on a precise and fast frequency detector that requires a high computational burden. Another disadvantage of OLS techniques lies in the fact that the implementation involves the calculation of sine and cosine functions, which are a drawback when digital implantation on a low cost is required [35].

The main aim of this paper is to design an efficient OLS technique with a very fast dynamic response, efficient operation at nominal and non-nominal frequencies, high filtering capacity, structural simplicity, and unconditional stability. The contribution of the paper is a new OLS called M-STFs-ADALINE. It is organised in two main blocks: the first block is a new technique to extract and separate the positive and negative sequence under highly unbalanced and distorted voltage. This OLS is characterised by its flexibility and ability to be simplified under some specified conditions. This simplified form is called a decoupled double self-tuning filter (DDSTF). Another advantage can also be noticed: the dc offset rejection capability, which is not the case for the majority of grid synchronizations. The second block is the frequency detector that is a simple neural approach to achieve the grid frequency adaptation online. Unlike the existing frequency estimators, this technique is motivated by its implementation simplicity and the immunity to the voltage signal amplitude and phase variation or disturbances. A pre-filtering stage is introduced to overcome the problem of harmonics. Experimental verification was performed to show the high performance and robustness of the proposed OLS even under the harsh environment such as low voltage ride through operation (LVRT).

II. Background

A. Grid Voltage Definition

It is considered that the three-phase voltage signal, originally in three-phase coordinates has been transformed to fixed frame (α, β) coordinates using the following Clarke's transformation

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{\sqrt{2}}{3} \begin{bmatrix} 1 & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}. \quad (1)$$

The phase angle can be obtained by:

$$\theta = \omega t = \tan^{-1}(V_\beta, V_\alpha), \tag{2}$$

where θ is the four-quadrant angle because the function returns the correct values even if the angular frequency is time-varying, just as long as the grid is balanced and not disturbed with harmonics.

$$V_\alpha = \sum_{h=0}^{\infty} V_h^p \cos(h\omega t + \phi_{ph}) + V_h^n \cos(h\omega t + \phi_{nh}), \tag{3}$$

$$V_\beta = \sum_{h=0}^{\infty} V_h^p \sin(h\omega t + \phi_{ph}) - V_h^n \sin(h\omega t + \phi_{nh}), \tag{4}$$

where V_h^p, V_h^n are h harmonic RMS values of positive and negative sequences, respectively; ϕ_{ph} and ϕ_{nh} are the sequences phases.

B. Q-OLS Estimator (Self-Tuning Filter)

The following synchronous reference frame will be studied [37]:

$$\hat{V}_{\alpha\beta}^{+}(t) = e^{j\omega t} \int e^{j\omega t} V_{\alpha\beta}(t) dt, \tag{5}$$

where $\hat{V}_{\alpha\beta}^{+}(s)$ and $V_{\alpha\beta}(s)$ are the instantaneous signals, respectively before and after integration in the synchronous reference frame. The previous equation can be expressed by the following transfer function with the Laplace transformation:

$$H(s) = \frac{\hat{V}_{\alpha\beta}^{+}(s)}{V_{\alpha\beta}(s)} = \frac{s + j\omega}{s^2 + \omega^2}. \tag{6}$$

In [37], [38], authors introduced a constant k in the transfer function $H(s)$ to obtain an STF with a cut-off frequency so that the previous transfer function $H(s)$ becomes

$$H(s) = k\frac{(s+k) + j\omega_c}{(s+k)^2 + \omega_c^2} = \frac{k[(s+k) + j\omega_c]}{[(s+k) + j\omega_c][(s+k) - j\omega_c]}, \tag{7}$$

$$\frac{\hat{V}_{\alpha\beta}^{+}}{V_{\alpha\beta}} = \frac{k}{(s - j\omega_c) + k}, \tag{8}$$

where

$$\hat{V}_{\alpha\beta}^{+}(s) = \hat{V}_\alpha^{+} + j\hat{V}_\beta^{+}, \; V_{\alpha\beta}(s) = V_\alpha(s) + jV_\beta(s).$$

One can notice that the complex operator j is achieved using the cross-coupling between the (αβ) axes. The block diagram of the STF tuned at the pulsation is depicted in Fig. 1.

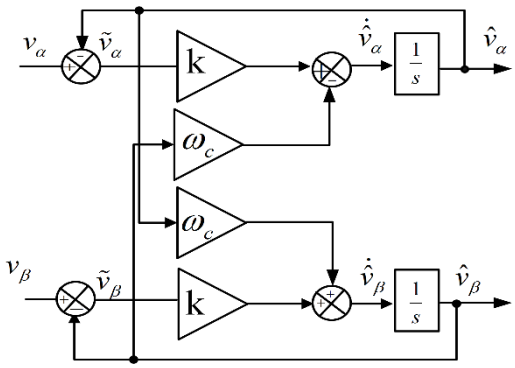

Fig. 1. Block diagram of the STF.

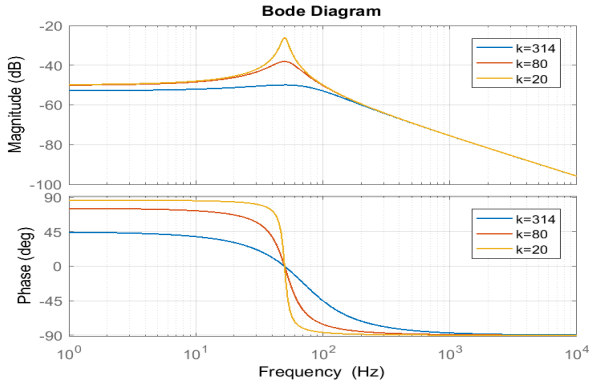

Fig. 2. Bode diagram of the STF.

Figure 2 shows the frequency response of (8) for $\omega_c = 314$ rad/s and three value of k. The response of the negative frequencies in these plots can be interpreted as the response to negative sequence vector signal. The frequency response is asymmetrical around zero and the gain is one with zero phase shifts at the fundamental of positive sequence while it provides a certain level of attenuation at the same frequency in the negative sequence. The dynamic response depends on the parameter k. A detailed study is given in [38].

C. STF Shortcomings

The STF suffers from two main shortcomings. Firstly, the STF can only attenuate but not eliminate the effect of the fundamental negative sequence components of the grid voltages. Secondly, the disturbances related to the utility frequency variation are not taken into account.

III. The Proposed Q-OLS Technique

Figure 3 illustrates the proposed Q-OLS technique. The key part of this structure is the DD-M-STFs that extract and separate the grid voltage positive and negative sequence. The extracted positive sequence is subtracted from the grid voltage signal and passed through a low-pass filter (LPF) to give estimation of the dc component. As the DD-M-STFs centre frequency is not adaptive (fixed at the nominal frequency) an ADALINE neural net enhanced by a pre-filtering stage is used to achieve the grid frequency adaptation online.

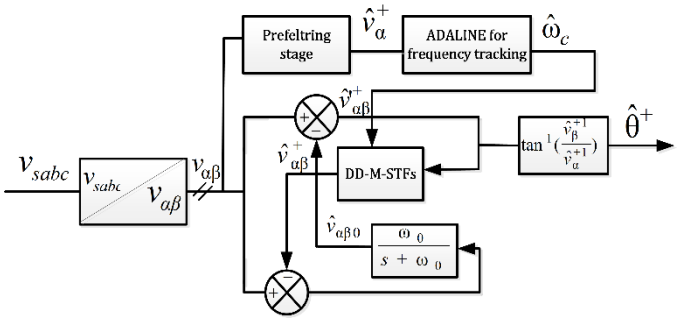

Fig. 3. The proposed synchronization technique.

A. Synchronization Structure Selection for the Extraction of the Positive and Negative Sequence

This subsection provides a new technique to extract the fundamental positive and negative sequence. As shown in Fig. 3, the frequency response is asymmetrical around zero, which allows distinguishing the negative polarities from the positive ones for the same frequency. The transfer function for obtaining the positive sequence is given in (8) and the negative sequence is as follows:

$$\frac{\hat{V}_{\alpha\beta}^{-}}{V_{\alpha\beta}}=\frac{k}{(s+j\omega_c)+k}. \tag{9}$$

For the sake of simplicity, the M-STFs is considered to be composed of only two STFs tuned at the positive and negative sequence of the fundamental frequency voltage.

The two STFs can provide accurate detection of the fundamental frequency positive sequence (FFPS) and fundamental frequency negative sequence (FFNS) under unbalanced yet not distorted (or slightly distorted) grid conditions. This method is named the decoupled double STF (DDSTF) and its implementation block diagram is shown in Fig. 4.

The DDSTF structure can be expressed with a set of frequency-domain equations:

$$\begin{cases}\hat{V}_{\alpha}^{+}(s)=\dfrac{k}{s-jn\omega_c+k}[V_{\alpha}(s)-\hat{V}_{\alpha}^{-}(s)]\\ \hat{V}_{\beta}^{+}(s)=\dfrac{k}{s-jn\omega_c+k}[V_{\beta}(s)-\hat{V}_{\beta}^{-}(s)]\\ \hat{V}_{\alpha}^{-}(s)=\dfrac{k}{s+jn\omega_c+k}[V_{\alpha}(s)-\hat{V}_{\alpha}^{+}(s)]\\ \hat{V}_{\beta}^{-}(s)=\dfrac{k}{s+jn\omega_c+k}[V_{\beta}(s)-\hat{V}_{\beta}^{+}(s)]\end{cases}, \tag{10}$$

where $\hat{V}_{\alpha}^{+}(s)$, $\hat{V}_{\beta}^{+}(s)$ and $\hat{V}_{\alpha}^{-}(s)$, $\hat{V}_{\beta}^{-}(s)$ are the estimated positive and negative sequences of V_{α} and V_{β}, ω_c is the cut-off frequency of the DDSTF.

$$\begin{cases}\hat{V}_{a0}(s)=\dfrac{\omega_0}{s+\omega_0}[V_{\alpha}(s)-\hat{V}_{\alpha}^{+}(s)-\hat{V}_{\alpha}^{-}(s)]\\ \hat{V}_{\beta0}(s)=\dfrac{\omega_0}{s+\omega_0}[V_{\beta}(s)-\hat{V}_{\beta}^{+}(s)-\hat{V}_{\beta}^{-}(s)]\\ \hat{V}_{\alpha}^{+}(s)=\dfrac{k}{s-jn\omega_c+k}[V_{\alpha}(s)-\hat{V}_{\alpha}^{-}(s)-\hat{V}_{\alpha0}^{-}(s)]\\ \hat{V}_{\beta}^{+}(s)=\dfrac{k}{s-jn\omega_c+k}[V_{\beta}(s)-\hat{V}_{\beta0}^{+}(s)-\hat{V}_{\beta}^{-}(s)]\\ \hat{V}_{\alpha}^{-}(s)=\dfrac{k}{s+jn\omega_c+k}[V_{\alpha}(s)-\hat{V}_{\alpha}^{+}(s)-\hat{V}_{\alpha0}]\\ \hat{V}_{\beta}^{-}(s)=\dfrac{k}{s+jn\omega_c+k}[V_{\beta}(s)-\hat{V}_{\beta}^{+}(s)-\hat{V}_{\beta0}]\end{cases} \tag{11}$$

B. DC Offset Removal Using DDSTF

The removal of the dc offset in the DDSTF input is shown in Fig. 3. To achieve an estimation of the dc component, the extracted FFPS is subtracted from the grid voltage signal and passed through the LPF, where $V_{\alpha0}$, $V_{\beta0}$ are the DC components of V_{α} and V_{β} in stationary reference frame.

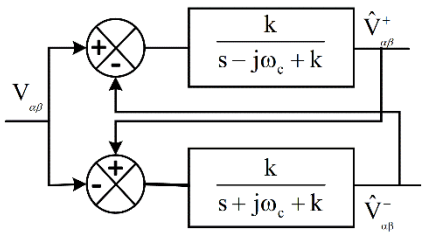

Fig. 4. Block diagram of the DDSTF structure.

C. Synchronization Structure for Highly Distorted Source Voltage

Under highly distorted source voltage, the performance of DDSTF can be improved by adding extra STFs tuned at harmonic frequencies. For example, n = +1, −1, −5, 7. This technique is named M-STFs. The M-STFs structure can be expressed with a set of frequency-domain as follows:

$$\begin{cases} \hat{V}^{+}_{\alpha n}(s)=\dfrac{k}{s-jn\omega_c+k}[V_\alpha(s)+\hat{V}^{+}_{\alpha n}(s)-\sum_{x=1}^{n}\hat{V}^{+}_{\alpha x}(s)-\sum_{y=-1}^{-n}\hat{V}^{-}_{\alpha y}(s)] \\ \hat{V}^{+}_{\beta n}(s)=\dfrac{k}{s-jn\omega_c+k}[V_\beta(s)+\hat{V}^{+}_{\beta n}(s)-\sum_{x=1}^{n}\hat{V}^{+}_{\beta x}(s)-\sum_{y=-1}^{-n}\hat{V}^{-}_{\beta y}(s)] \\ \hat{V}^{-}_{\alpha n}(s)=\dfrac{k}{s+jn\omega_c+k}[V_\alpha(s)+\hat{V}^{-}_{\alpha n}(s)-\sum_{x=1}^{n}\hat{V}^{+}_{\alpha x}(s)-\sum_{y=-1}^{-n}\hat{V}^{-}_{\alpha y}(s)] \\ \hat{V}^{-}_{\beta n}(s)=\dfrac{k}{s+jn\omega_c+k}[V_\beta(s)+\hat{V}^{-}_{\beta n}(s)-\sum_{x=1}^{n}\hat{V}^{+}_{\beta x}(s)-\sum_{y=-1}^{-n}\hat{V}^{-}_{\beta y}(s)] \end{cases}. \quad (12)$$

D. Grid Frequency Estimation

An ADALINE neural net for frequency estimation was introduced in [13].

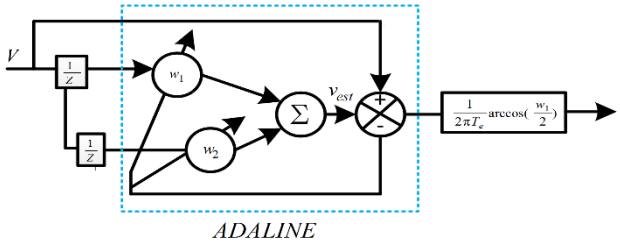

Fig. 5. ADALINE for frequency estimation.

This approach has been used to identify the voltage parameters given by

$$V(k)=\sum_{n=1}^{\infty}A_n\sin(\omega_n kT_e+\phi_n), \quad (13)$$

where A_n, ω_n, and ϕ_n are the amplitude, pulsation, and phase of the n-th term, respectively. The recursive expression of $V(k)$ can be deduced as follows:

$$V(k+1)+V(k-1)=\sum_{n=1}^{\infty}A_n\sin(\omega_n kT_e+\phi_n)2\cos(\omega_n T_e)= \\ =2\cos(\omega_n T_e)V(k). \quad (14)$$

If the harmonics are neglected, the voltage signal $V(k)$ can be written as

$$V(k)=2\cos(\omega_1 T_e)V(k-1)-V(k-2). \quad (15)$$

Figure 5 illustrates this technique: the ADALINE has $V(k-1)$ and $V(k-2)$ as inputs and w_1, w_2 like weights; these weights will be adapted and converge toward the values −1 and −2, respectively. The voltage signal frequency is reconstructed online from the weight:

$$f=\frac{1}{2\pi T_e}\arccos\left(\frac{w_1}{2}\right). \quad (16)$$

E. Evolution of the Proposed Frequency Estimator under Distorted Source Voltage

The proposed method is not really adequate with respect to the presence of harmonics. As a solution, we introduce the STF in a stationary reference frame as a pre-filtering stage. This can be seen in Fig. 3. The analytical form of Eq. (8) is given by the following expressions.

$$\hat{V}_\alpha=\frac{\sqrt{3}}{2}\sum_{h=-\infty}^{+\infty}\frac{V_h}{1+\left(\frac{(1-h)\omega}{k}\right)^2}\begin{bmatrix}\sin\left[h\omega t+\varphi_h+\tan^{-1}\left(\frac{(1-h)\omega}{k}\right)\right] \\ -e^{kt}\sin\left[h\omega t+\varphi_h+\tan^{-1}\left(\frac{(1-h)\omega}{k}\right)\right]\end{bmatrix}\hat{V}_\beta \quad (17)$$

$$\hat{V}_\beta=\frac{\sqrt{3}}{2}\sum_{h=-\infty}^{+\infty}\frac{V_h}{1+\left(\frac{(1-h)\omega}{k}\right)^2}\begin{bmatrix}\cos\left[h\omega t+\varphi_h+\tan^{-1}\left(\frac{(1-h)\omega}{k}\right)\right] \\ -e^{kt}\sin\left[h\omega t+\varphi_h+\tan^{-1}\left(\frac{(1-h)\omega}{k}\right)\right]\end{bmatrix}\hat{V}_\alpha \quad (18)$$

From Eqs. (17) and (18), the total harmonic distortion of the fundamental component is:

$$THD\%=\frac{\sqrt{\sum_{h=2}^{n}\left(\frac{V_h}{\sqrt{1+\left[\frac{(1-h)\omega}{k}\right]^2}}\right)^2}}{V_1}. \quad (19)$$

From Eq. (19), it is clear that by taking k small, the harmonic cancelation becomes better, but according to the exponential part in (17) and (18), the transient time becomes too large. The STF performance is the result of a trade-off between an excellent harmonic cancelation and a good transient response. By choosing k (STF) = 80, the transient time is 0.02 s and Eqs. (17) and (18) become:

$$\hat{V}_\alpha=\frac{\sqrt{3}}{2}(1-e^{-kt})\sin(\omega t+\varphi), \quad (20)$$

$$\hat{V}_\beta=\frac{\sqrt{3}}{2}(1-e^{-kt})\cos(\omega t+\varphi). \quad (21)$$

IV. Simulation Results

The proposed algorithm is simulated using MATLAB/Simulink. Three scenarios are investigated: frequency variation unbalanced and distorted with the presence of dc offset in voltage in order to analyse the performance and the effectiveness of the proposed algorithm.

A. Robustness of Frequency Estimator

To verify the robustness of the frequency estimator, three tests are respectively shown in Fig. 6. It consists in variation under ideal condition, under unbalanced and distorted source voltage and finally under unbalanced, distorted and DC offset source voltage (at 0.08 s, the frequency jumped from 50 Hz to 45 Hz). Moreover, these tests are compared with other recent methods such as the DDSTF-PLL.

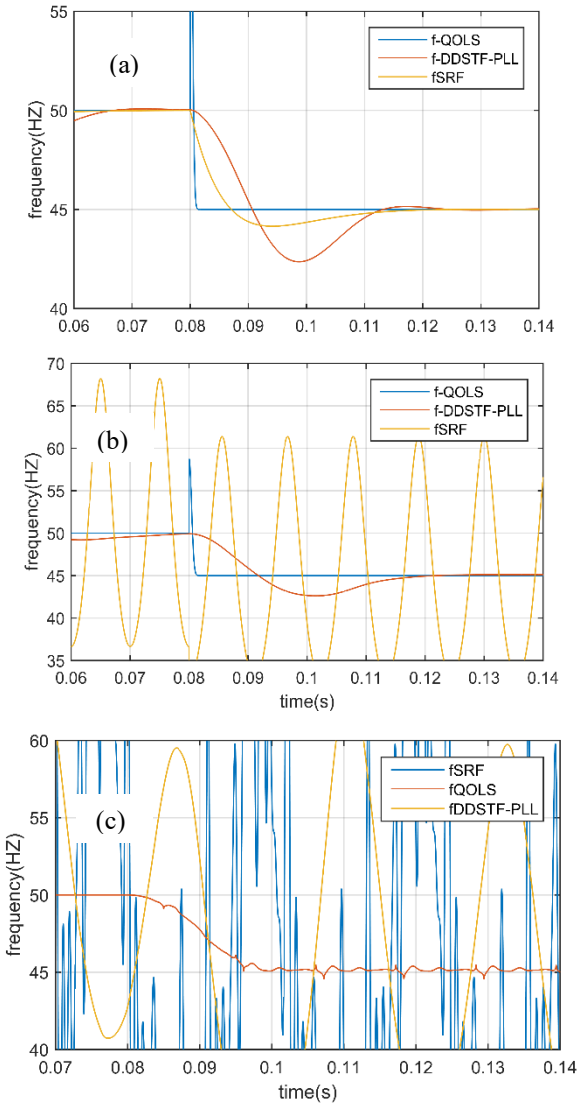

Fig. 6. Simulation results under supply frequency change: (a) frequency change under an ideal condition, (b) frequency change under a highly unbalanced and distorted condition, (c) variation of the frequency under a highly unbalanced, distorted and DC offset.

According to this figure, the following observations are made: 1) the proposed frequency estimator benefits from very fast dynamic response; 2) immunity and efficiency under highly unbalance and distorted and dc offset and which is not the case of the DDSTF-PLL [41] and SRF-PLL; 3) in Fig. 6 (c) the pre-filtering stage in the Q-OLS affects slightly (less than one period) the dynamic of the Q-OLS.

B. Highly Unbalanced Source Voltage

40 % of unbalanced source voltage is introduced in the main voltages. Besides, at 0.08 s, the frequency jumped from 50 Hz to 45 Hz.

According to Fig. 7, the proposed Q-OLS and DDSTF-PLL converge to similar results; the main advantage of the Q-OLS is the fastest dynamic response thanks to the frequency estimator.

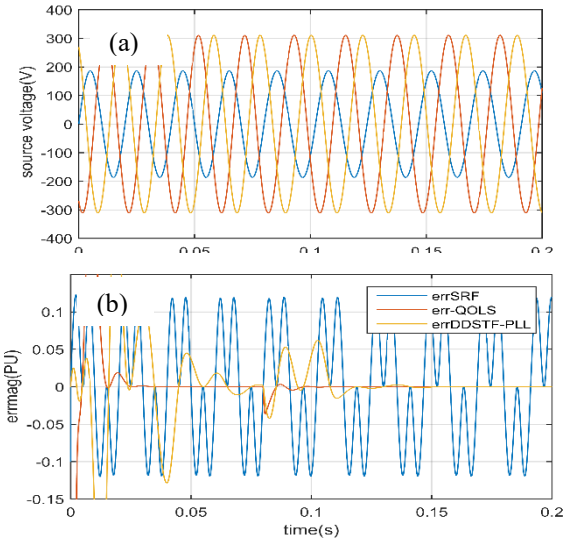

Fig. 7. Simulation results under highly unbalance and frequency change: (a) three-phase source voltages; (b) magnitude error of three-phase unit voltages.

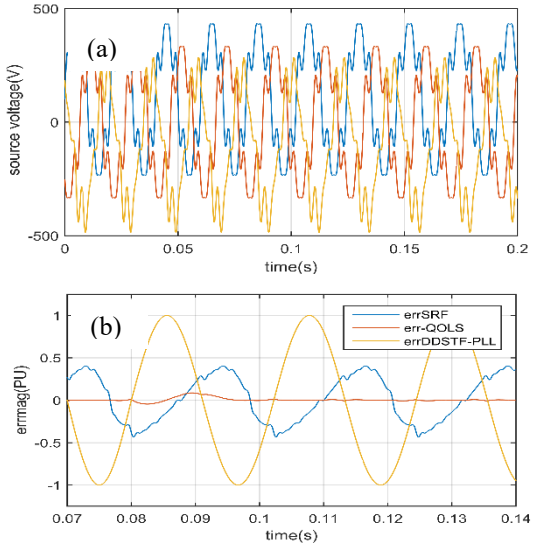

Fig. 8. Simulation results under distorted and DC offset with frequency change: (a) three-phase source voltages; (b) magnitude error of three-phase unit voltages.

C. Highly Distorted Source Voltage and DC Offset

In this scenario, we simulate the distorted voltage with the THD of 30 %. In addition, a DC component of phase a (+100 V) and phase c, (−100 V) is added to the grid voltages. Under this test, the frequency jumped from 50 Hz to 45 HZ.

According to Fig. 8, the proposed Q-OLS is largely better than the DDSTF-PLL and the SRF-PLL. Another advantage of the Q-OLS is the fastest dynamic response thanks to the frequency estimator.

V. Experimental Results

This section provides some experimental results to evaluate the performance of the synchronization techniques, the proposed Q-OLS (DDSTF-ADALINE) and the Q-OLS combined with PLL (DDSTF-PLL). A dSpace 1104 processing

board with a sampling frequency of 10 kHz hosts the implementation of the proposed algorithms. First, a test signal will be generated digitally using the processor embedded in the dSpace 1104. Then a digital to analogue converter is used to convert the generated signal to an analogue signal. The obtained analogue signal emulates a real world measured voltage signal. At the third stage, the analogue signal is acquired and converted to a digital signal. The resulting signal, which virtually represents a measured voltage, is provided to the synchronization algorithm. To have a reference for comparison, the conventional (SRF-PLL) is also implemented. The parameters of the system are listed in Table I.

TABLE I

TEST SCENARIO PARAMETERS

Component	Magnitude [P.U.]	Phase [deg.]
Positive sequence	0.733	5°
Negative sequence	0.4	50.4°
3rd harmonic	0.1	90°
5th harmonic	0.1	45°
7th harmonic	0.07	180°
11th harmonic	0.3	180°

A. Frequency Variation

Figure 9 demonstrates the obtained results in response to a 5 Hz frequency step change. The frequency jumps from 50 Hz to 45 Hz. As it can be observed, alongside the SRF-PLL the DDSTF-ADALINE has the fastest dynamic response. It implies the efficiency of the proposed frequency estimator.

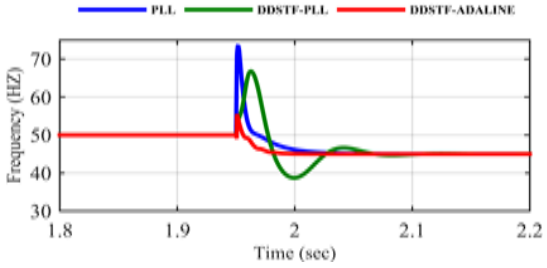

Fig. 9. Experimental results under supply frequency change.

B. Highly Unbalance Source Voltage

Nominal and off-nominal grid frequency is carried in this test to verify the robustness of the synchronization technique against the grid frequency fluctuations.

Figures 10 and 11 show the obtained results under a highly unbalanced grid condition. Based on these results, the following observations are made: 1) the proposed OLS technique totally rejects the grid voltage unbalance under nominal and off-nominal frequencies by accurately extracting the positive and the negative sequence with a fast-dynamic response; 2) the SRF-PLL is not affected by the grid frequency changes and it suffers from rather large oscillatory ripples in both nominal and off-nominal frequencies.

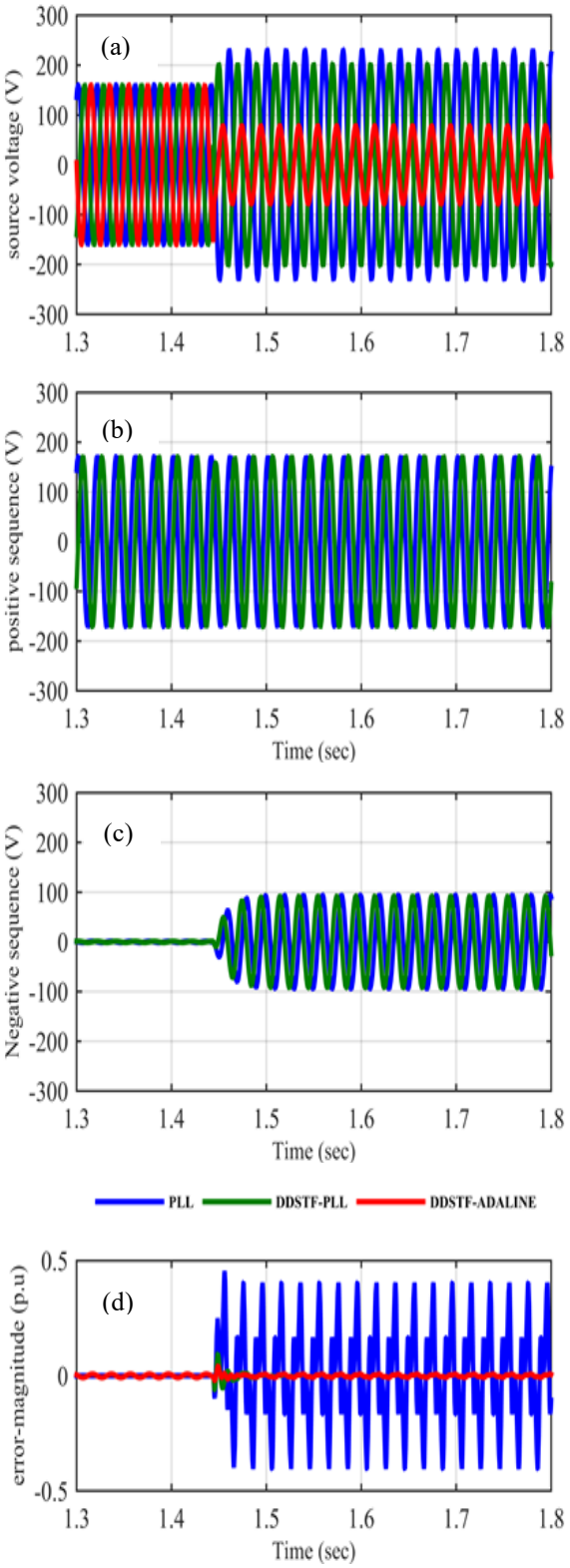

Fig. 10. Experimental results under highly unbalance source voltage: (a) three-phase source voltage, (b) positive sequence voltage (DDSTF-ADALINE), (c) negative sequence voltage (DDSTF-ADALINE), (d) error magnitude.

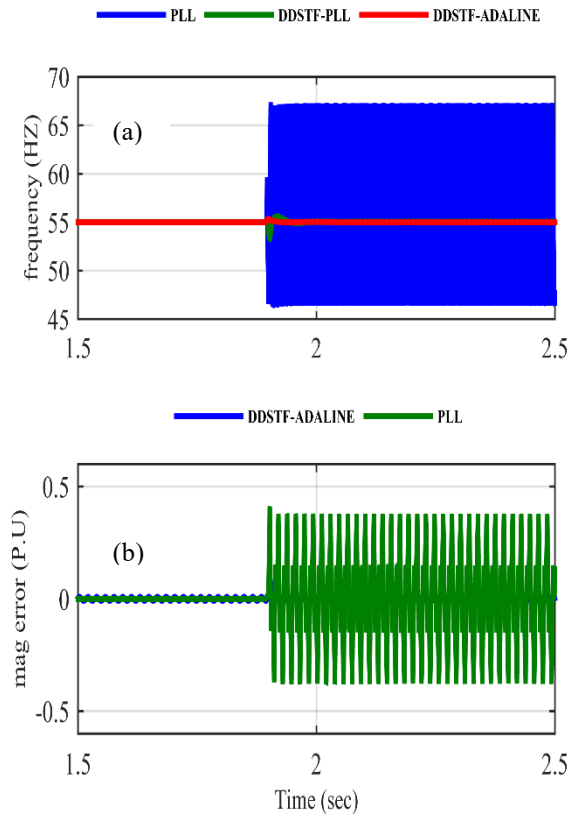

Fig. 11. Experimental results under highly unbalance source voltage: (a) estimated frequency, (b) magnitude error.

C. Distorted Source Voltage

Figure 12 shows the experimental results under distorted source voltage. From this figure, it clear that the proposed OLS technique totally rejects the harmonics and the frequency is estimated precisely thanks to the filtering stage.

D. Presence of the DC Offset in the Grid Voltage

In this scenario, a dc component of phase (a) and phase (c) +100 V, −100 V is added to the grid voltages.

Figure 13 shows the experimental results under dc offset. It is clear that the dc offset is completely rejected by the DDSTF-ADALINE and it is not the case for the SRF-PLL and the DDSTF-PLL.

E. LVRT Case

This test is carried out to highlight the performance of our synchronization technique, and for the sake of the verification it is compared with the M-STFs- PLL and the SRF-PLL.

The application performance test highlights the M-STFs ADALINE contribution to the LVRT requirements of the grid codes (Fig. 14).

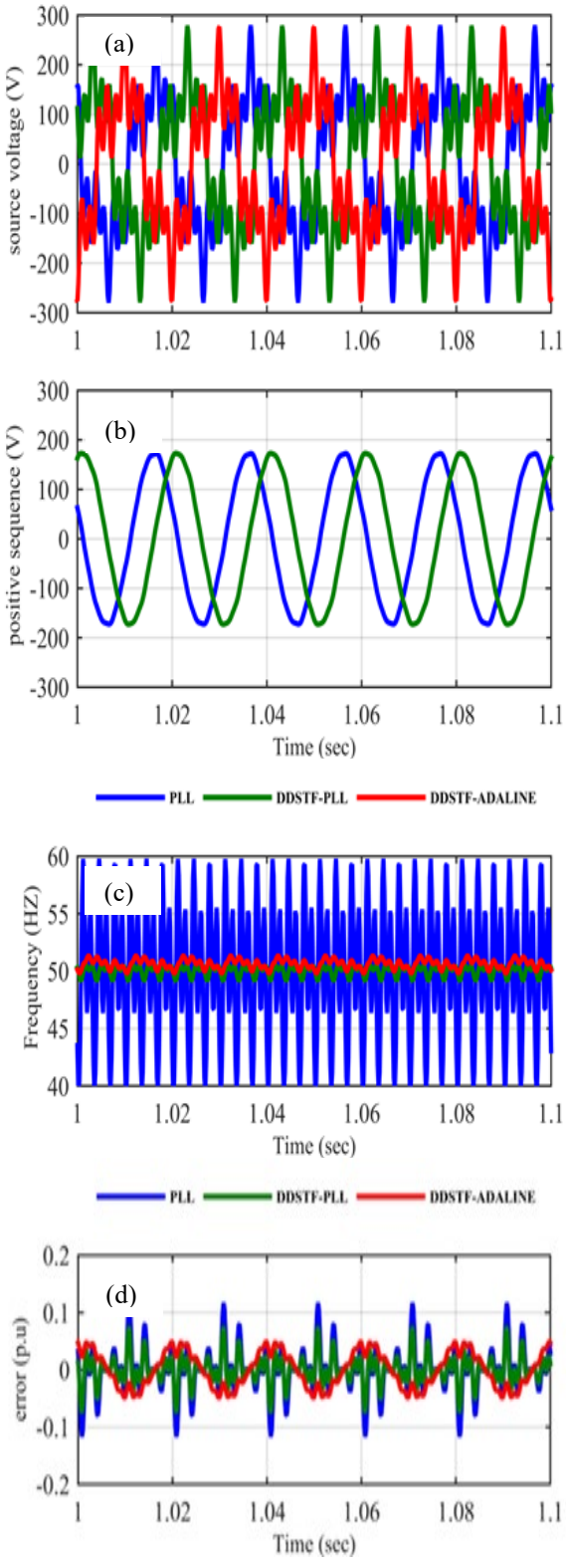

Fig. 12. Experimental results under distorted source voltage: (a) three-phase source voltage, (b) positive sequence voltage (M-STF-ADALINE), (c) estimated frequency, (d) error magnitude.

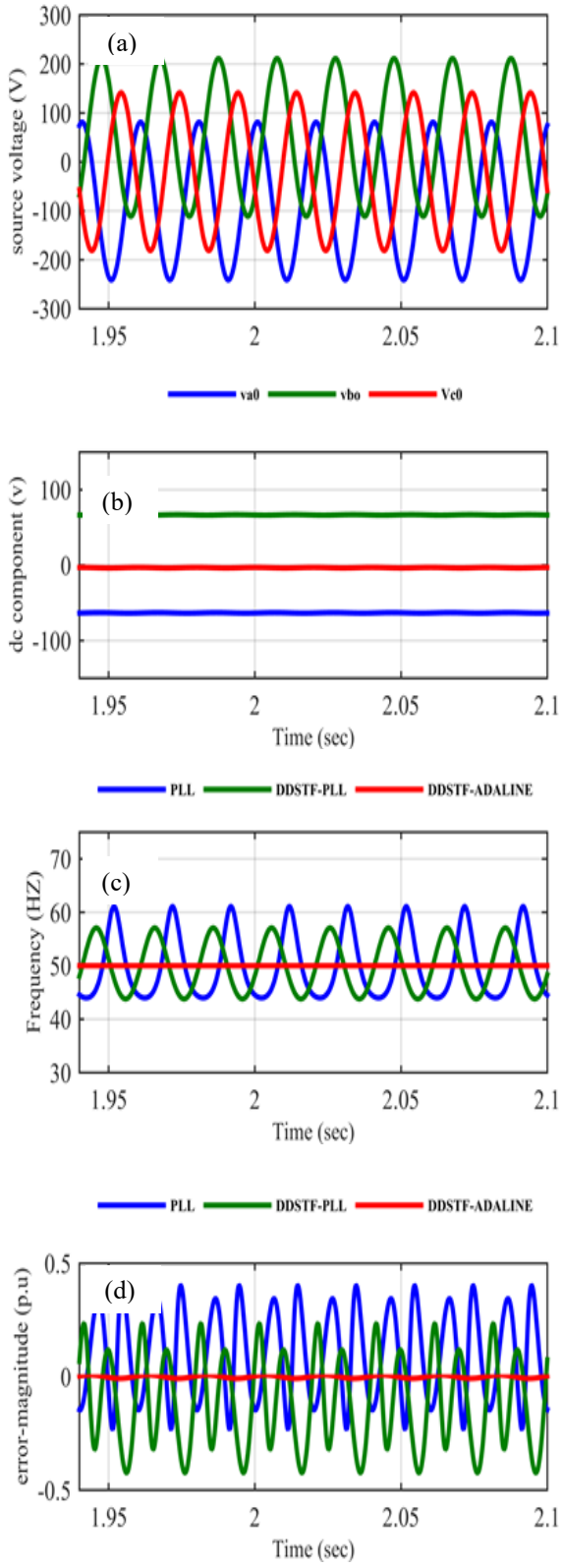

Fig. 13. Experimental results under dc offset: (a) three-phase source voltage, (b) DC component, (c) estimated frequency, (d) error magnitude.

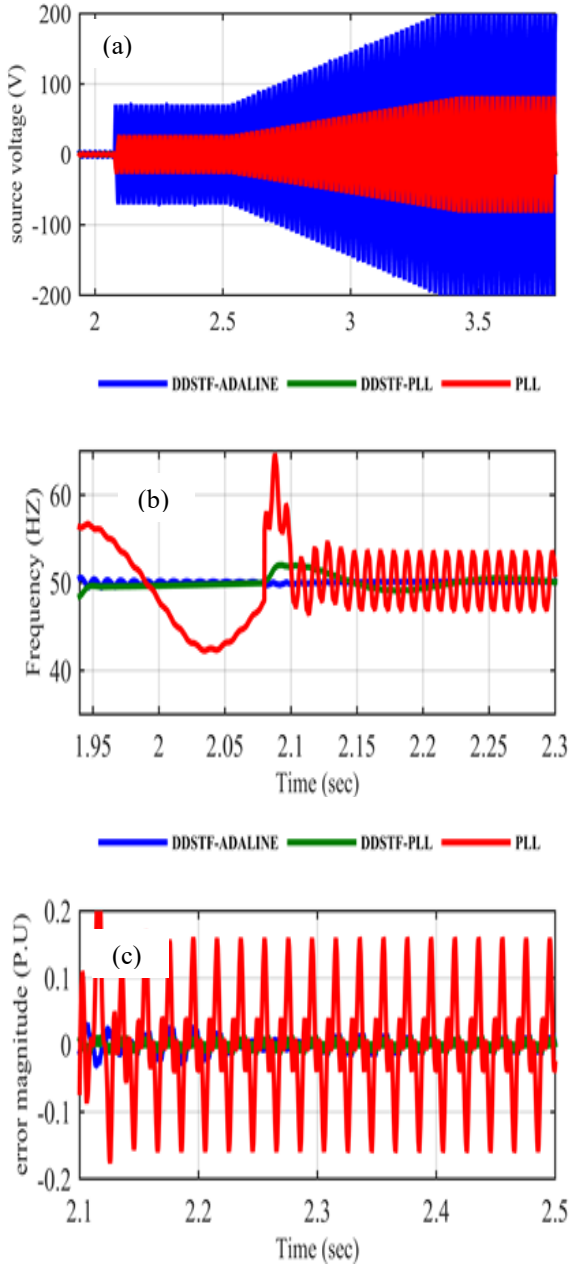

Fig. 14. Experimental results under LVRT: (a) source voltage, (b) estimated frequency, (c) error magnitude.

VI. Summary of Comparison

This subsection provides a comparison study of the DD- M-STFs-ADALINE based method with the SRF-PLL, DSOGI-FLL, DD-M-STFs-PLL and the POLS. The methods are compared according to the following standpoints: unbalance robustness, frequency adaptability, distortions, DC offset, structural simplicity (ease of design, tuning and implementation). Table II presents the magnitude error under such circumstances.

A. Unbalance Robustness

According to Table II, the DDSTF-ADALINE and DDSTF-PLL converge to similar results. It is clear that the proposed DDSTF-ADALINE outperforms the POLS and is largely better than the SRF-PLL. The main advantage of the proposed DDSTF algorithm comparing with DSOGI is the extraction of positive and negative sequence with no need of symmetrical component.

B. Frequency Adaptability

Table III gives a brief comparison of transient responses under frequency steps. In Table III, it can be noticed that the DSOGI, the DD-M-STFs-PLL, and POLS have a longer response time; the proposed DD-M-STFs-ADALINE and the SRF-PLL have the fastest dynamic response. Nevertheless, the SRF-PLL cannot deal with unbalance.

C. Distortion

Under distorted source voltage, the M-STFs-ADALINE and the POLS converge to similar results. On the other hand, it can be noticed that the proposed M-STF is more efficient than the conventional SRF-PLL and the DSOGI-FLL (Table II). Under highly distorted source voltage, the performance of DSOGI can be improved by adding extra SOGIs (tuning at the harmonic frequencies) and a harmonic decoupled network (HDN). However, it has a very heavy computational load (26 µs, see Table IV). On the contrary, the M-STFs-ADALINE is executed in 4 µs.

D. DC Offset Rejection

Table II compares the performances of the DDSTF-ADALINE, SRF-PLL, DDSTF-PLL, DSOGI-FLL and the POLS in the presence of overly large DC offset component. In this table, it can be seen that only the proposed M-STF-ADALINE technique demonstrates an excellent DC offset rejection capability.

E. Structural Simplicity

Table IV provides the execution time required by the proposed algorithm and by the other algorithms. We can see that the M-STFs-ADALINE and the DSOGI-FLL have similar execution time. Among all the aforementioned synchronization techniques, the POLS is the fastest synchronizer. On the other hand, the proposed M-STFs-ADALINE is fast compared to other advanced synchronization techniques, such as hybrid synchronous/stationary reference frame filtering based PLL [18] and the weighted least square phase estimation algorithm [19].

TABLE II

MAGNITUDE ERROR [P.U.] OBTAINED BY THE PROPOSED METHOD AND OTHER METHODS UNDER DIFFERENT TEST CONDITIONS

Error [P.U.]	DD-M-STFs-ADALINE	DD-M-STFs-PLL	SRF-PLL	DSOGI-FLL	POLS
Unbalance	0.004	0.005	0.4	0.007	0.15
Distortion	0.04	0.08	0.12	0.12	0.04
DC offset	0.004	0.2	0.4	0.4	0.4
LVRT	0.004	0.005	0.2	0.007	0.15

TABLE III

RESPONSE TIME COMPARISON

Method	Time response
DD-M-STFs-ADALINE	<20 ms
SRF-PLL	>20 ms
POLS	<40 ms [41]
DD-M-STFs-PLL	>40 ms
DSOGI	>40 ms

TABLE IV

RELATIVE EXECUTION TIME OF THE SYNCHRONIZATION METHODS

Method	Execution Time
POLS	1.72 µs
M-STF-ADALINE	4 µs
DSOGI-FLL	4 µs
LPN-PLL	7.9 µs
HPLL	9.69 µs
SRF-PLL	10 µs
EGDSC-PLL	10.63 µs
WLSE-PEA	13 µs
M-STFs-PLL	20 µs
M-SOGI-FLL	26 µs

VII. CONCLUSION

In this paper, a new quasi open-loop synchronization technique for grid-connected power converters applications has been presented. It is well suited to work under LVRT operation and is based on the self-tuning filter concept. The proposed method named DD-M-STFs-ADALINE is composed of two fundamental blocks. In the first block, the DDSTF algorithm cleanly extracts and separates the positive and negative sequences under some specified condition with no need for the symmetrical components and/or signal delay. Under highly distorted condition, this structure is enhanced by one STF tuned at each higher-order harmonic frequency (M-STFs). In the second block, an ADALINE network accurately achieves grid frequency adaptation online. The key features of the proposed

method are the following. 1) the proposed method is unconditionally stable; 2) it does not require the calculation of sine and cosine functions which is of a great advantage; 3) it has a fast-dynamic response; 4) efficient operation under nominal and off-nominal frequencies; 5) high filtering capability. An additionally interesting feature can also be noticed, the proposed method demonstrates good dc offset rejection capabilities and this is not the case of the main grid synchronization techniques. Experimental results have been obtained and show that the DD-M-STFs ADALINE is a very suitable synchronization technique for grid connected power converter applications especially for LVRT operations.

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