10.2478/v10144-009-0022-2

Analysis and Design of 3.3 kV IGBT Based Three-Level DC/DC Converter with High-Frequency Isolation and Current Doubler Rectifier

Dmitri Vinnikov, Tanel Jalakas, Indrek Roasto
Tallinn University of Technology
dm.vin@mail.ee, tjalakas@yahoo.com, indrek.roasto@ttu.ee

***Abstract* - The paper presents the findings of a R&D project connected to the development of auxiliary power supply (APS) for the high-voltage DC-fed rolling stock applications. The aim was to design a new-generation power converter utilizing high-voltage IGBT modules, which can outpace the predecessors in terms of power density, i.e. to provide more power for smaller volumetric space. The topology proposed is 3.3 kV IGBT-based three-level neutral point clamped (NPC) half-bridge with high-frequency isolation transformer and current doubler rectifier that fulfils all the targets imposed by the designers. Despite an increased component count the proposed converter is very simple in design and operation. The paper provides an overview of the design with several recommendations and guidelines. Moreover, the simulation and experimental results are discussed and the performance evaluation of the proposed converter is presented.**

INTRODUCTION

Electric traction is one of the major present-day solutions for environmental problems. Electric traction is safe, economical, reliable and with a minimum environmental impact. The latest demands for energy efficient, reliable and safe rolling stock require new technologies for the design of power electronic converters in the railway applications. The auxiliary power supply converter (APS) is one of the basic systems used in rolling stock. It provides low-voltage power to every onboard electrical system and equipment on a rail vehicle, including those that are critical to its safety and operability (like brakes or lighting systems). In brief, APS represents a galvanically isolated step-down DC/DC converter, transforming high voltage from the traction catenary (3.0 kV DC in the case of a high-voltage DC catenary) to a lower voltage (350 V DC) for the onboard electric facilities. It is obvious that a failure within this system would render the whole vehicle non-operational, resulting in a financial loss, operational problems to the rolling stock owner and discomfort to passengers.

Regarding to the specific design rule, converters based on the IGBT technology for the catenary voltages of 3.0 kV DC are only possible with IGBTs with the blocking voltage not lower than 6.0 kV [1]. The new proposed topology (Fig. 1) utilizes the three-level concept of the input inverter. The three-level half-bridge topology can be easily derived from the two-level one with the series connected transistors by the introduction of clamping diodes, which balance out voltage sharing between series connected top and bottom group transistors. Moreover, to further improve the power density of the APS it was decided to implement the current doubler rectifier (CDR) on the output stage of the converter.

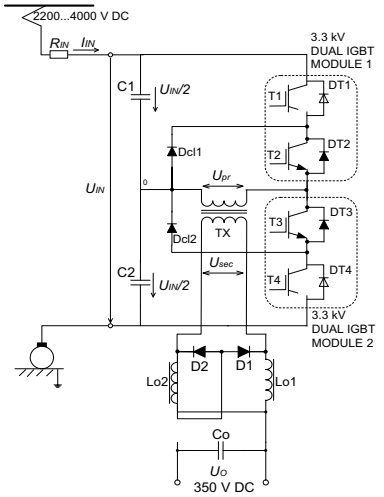


Fig. 1. Proposed three-level NPC half-bridge topology with high-frequency isolation and current doubler rectifier.

The three-level half-bridge converters have been analyzed and discussed in [2], [3], [4], [5], but these investigations were mostly connected with low power (≤ 8 kW) low-to-middle voltage (≤ 1.3 kV) applications. In this paper, first the three-level half-bridge isolated DC/DC converter topology will be evaluated for high-voltage (≥ 2 kV) high-power (≥ 10 kW) applications. The general specifications of the developed converter are submitted in Table I.

TABLE I
GENERAL SPECIFICATIONS OF THE DEVELOPED CONVERTER

Parameter	Value
Nominal input voltage, U_{in}	3.0 kV DC
Minimal input voltage, $U_{in,min}$	2.2 kV DC
Maximal input voltage, $U_{in,max}$	4.0 kV DC
Nominal output voltage, U_O	350 V DC
Rated output power, P_O	50 kW
Primary inverter switches (*T1, T2, T3, T4*)	2 x dual IGBT modules 3.3 kV 200 A (INFINEON FF200R33KF2C)
Switching frequency, f_{sw}	4000 Hz
Isolation transformer type	Vacuum impregnated toroidal transformer
Secondary rectifiers	Dual FRED modules DH2x61-18A

DESIGN AND OPERATION OF THE PROPOSED CONVERTER

The key specific feature of the catenary-fed rolling stock converters is that they must operate normally despite the widely changing input voltage. The boundaries of the input voltage are presented in Table I (minimal and maximal input voltages). In the normal steady-state operation of the transformer-isolated half-bridge converter, the relation $U_{in}D$ (where U_{in} is the input voltage and $D=t_{on}/T_{sw}$ is the transistor duty cycle) is constant. In converters with wide input voltage swing, to provide constant volt-seconds over the primary winding of the isolation transformer, the maximum duty cycle D_{max} must always be associated with the minimal input voltage $U_{in,min}$ and the minimum duty cycle D_{min} must correspond to the maximal input voltage $U_{in,max}$. The input voltages and the corresponding duty cycles of the developed converter are presented in Table II. Further analysis will mostly be based on these boundary operating points.

TABLE II
INVERTER OPERATING VOLTAGES AND CORRESPONDING DUTY CYCLES

Input voltage	$U_{in,min}$	$U_{in,max}$
	2.2 kV DC	4.0 kV DC
Duty cycle	D_{max}	D_{min}
	0.4	0.22

A. Three-Level Half-Bridge NPC Inverter

The operation of a three-level half-bridge NPC inverter can be divided to four operating modes - two conduction and two freewheeling modes. The first - the positive conduction mode - operates when T1 and T2 are on and T3 and T4 are off. In that mode the current flows from the catenary and through transistors T1, T2, the isolation transformer TX, and the capacitor C2. The second mode - the positive freewheeling mode - when T1 and T4 are off, T2 and T3 are on and Dcl1 is conducting. This mode is followed by the negative conduction mode (T1 and T2 are off and T3 and T4 are on) and the negative freewheeling mode (T1 and T4 are off, T2 and T3 are on and Dcl2 is conducting). The timing diagrams of inverter switches and the primary voltage waveform of the isolation transformer are presented in Fig. 2.

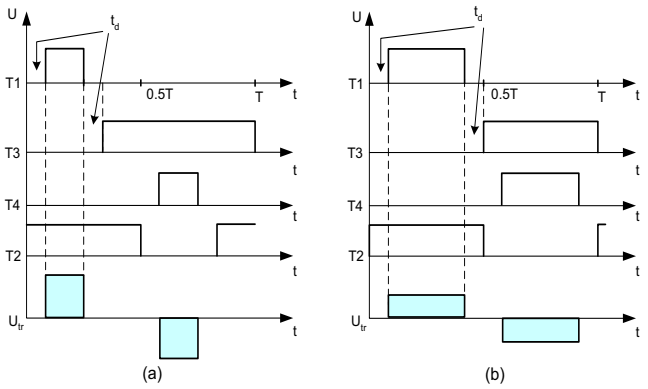


Fig. 2. Timing diagrams of the proposed three-level half-bridge NPC inverter: maximal input voltage and minimum duty cycle (a) and minimal input voltage and maximum duty cycle (b).

To achieve regulation of the output voltage the resulting duty cycle seen on the transformer primary is changing inversely proportional to the input voltage change. Neglecting losses and transients, the operating conditions of the inverter switches in the three-level configuration could be described as:

$$U_{CE,\max} = \frac{U_{in,\max}}{2}. \quad (1)$$

$$I_{C,\max} = \frac{P_O}{U_{in,\min} \cdot D_{\max}}. \quad (2)$$

Thus, each transistor in the three-level NPC topology is operating with half the input voltage and the same collector current as with the conventional two-level topology. This fact provides a possibility of faster 3.3 kV IGBT modules to be implemented, thus achieving higher power density of the converter (reduced heatsink requirements due to lower losses for the same switching frequency or reduced passive components due to increased switching frequency).

Theoretically, to control a three-level inverter, four PWM generators are needed. The external logic circuit presented in Fig. 3 allows the required number of independent PWM channels to be effectively reduced by two in cases of symmetric PWM control. The control is made very easy: outer transistors T1 and T4 are controlled directly from the PWM generators of a microcontroller, while inner switches T3 and T2 are drived by the inversions of the corresponding control PWM signals. These inversions are derived by the external inverter logic (NOT gate) realized by the logic IC - 74HT04 HEX inverter.

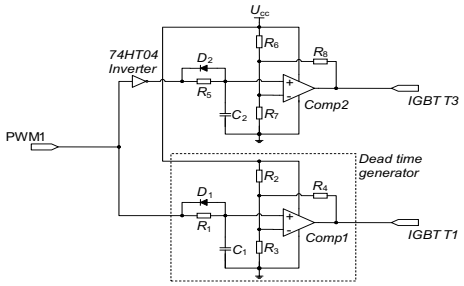


Fig. 3. Proposed control signal inverter circuit with an integrated dead time generator.

Since the IGBTs are not ideal switches and have a certain turn-on and turn-off delay times, a situation can occur where three devices T1, T2, T3 or T2, T3, and T4 are simultaneously conducting. Having three devices conducting at the same time would result in the short circuit of the corresponding input capacitor C1 or C2 and the IGBTs would be destroyed. In order to prevent short circuit, it is necessary to add a dead time t_d between the original and the inverted PWM signal, as shown in Fig. 2. For that purpose the special dead time generator was implemented in control circuitry of

each transistor (Fig. 3). A control pulse from the microcontroller sets the pin PWM1 high and the capacitor C1 will be charged over resistors R1 and R2. The comparator compares that voltage with its reference voltage and toggles the output if the reference voltage has been reached. If the PWM signal returns to low, then the capacitor C1 will be discharged over the diode D1 and the comparator toggles the output back to zero. The same dead time generator is implemented for the inverted control channel as well.

B. Isolation Transformer and Current Doubler Rectifier

To further improve the power density of the APS it was decided to implement the current doubler rectifier (CDR) on the output stage of the converter (Fig. 1). The main problems of the full-bridge rectifier (FBR) used in the previous design [1], were the increased losses of the transformer secondary winding due to high secondary current and the very high conduction losses of the rectifier bridge caused by the current having to go through two diodes in each half-cycle.

In contrast to the full-bridge rectifier, the current doubler topology inhibits several advantages: the total volume of the two filter inductors might be equal or even smaller than the inductor of the full-bridge due to their lower operating frequency and lower current ratings [6], [7]. Further tradeoffs can be made in order to reduce inductor sizes by lowering the inductance value and relying more strongly on the ripple current cancellation effect of the two inductors. Additionally, the current-doubler rectifier offers a potential benefit of better distributed power dissipation, which might become a vital benefit for the APS converters in terms of power density. The filter inductances can be estimated by (3).

$$L_{O1} = L_{O2} = \frac{U_O \cdot (1-D)}{\Delta I_L \cdot f_{sw}}, \tag{3}$$

where U_O is the output voltage, D is the operating duty cycle, ΔI_L is the inductor ripple current and f_{sw} is the switching frequency. In cases of electrolytic capacitors, the value of capacitance could be evaluated as:

$$C_O = \frac{80 \cdot 10^{-6} \cdot \Delta I_L}{\Delta U_O}, \tag{4}$$

where ΔU_O is the output ripple voltage.

The specificity of the CDR related to the isolation transformer is that the secondary winding's amplitude voltage $U_{sec,CDR}$ is twice as high as that of the full-bridge $U_{sec,FBR}$ used in previous design. Thus the current doubler transformer features doubled secondary turns number of the full-bridge one.

On the other hand, the secondary current of the isolation transformer is half the output current in case of CDR (5). Thus, the cross-section of a wire required for the secondary winding could be twice reduced in contrast to the full-bridge transformer (6).

$$I_{\sec(rms)CDR} = \frac{P_O}{2 \cdot U_O} \cdot \sqrt{2 \cdot D}\,. \tag{5}$$

$$I_{\sec(rms)FBR} = \frac{P_O}{U_O} \cdot \sqrt{2 \cdot D}\,. \tag{6}$$

Each inductor of the CDR topology conducts only half the output current, which in turn gives a possibility of reduced copper loss and better distributed power dissipation than with the full-bridge design. The rms inductor current of the CDR topology is:

$$I_{Lo(rms)} = \sqrt{\left(\frac{P_O}{2 \cdot U_O}\right)^2 + \frac{\left(\frac{P_O}{U_O} \cdot K_{ri}\right)^2}{12} \cdot \left(\frac{1-D}{1-2 \cdot D}\right)^2} = \tag{7}$$
$$= \frac{P_O}{2 \cdot U_O} \cdot \sqrt{1 + \frac{K_{ri}^2}{3} \cdot \left(\frac{1-D}{1-2 \cdot D}\right)^2},$$

where K_{ri} is the output current ripple factor.

In contrast to the full-bridge rectifier where the single inductor is operating at double the switching frequency, the inductors in CDR are operating at two times lower frequency and with the higher current ripple ΔI_L, thus requiring more inductance for the same output current ripple ΔI_O. In some cases, where the frequency response does not matter, it is more feasible to damp the output current ripple by adding extra capacitance to the output filter, thus minimizing demands for inductance.

ANALYSIS OF SIMULATIONS AND EXPERIMENTAL RESULTS

A. Simulation Results

The *Simplorer* simulation model of the developed three-level half-bridge DC/DC converter used in the analysis is shown in Fig. 4. The point of interest during the simulations was the operating conditions of the high-voltage IGBTs with the presented control algorithm. The switching frequency is 4 kHz. The input capacitors C1 and C2 are identical. In order to simplify the simulation, ideal semiconductor devices and a non-saturable isolation transformer were used. The leakage inductance of the primary winding was set at 5 μH, which corresponds to the parameter of the real isolation transformer developed for the project. The simulations were performed at the rated load conditions (i.e. with the constant output power 50 kW) and in two boundary operating points described above.

It was stated during the simulations that if the leakage inductance of the isolation transformer is relatively small (2-5 μH), zero voltage switching (ZVS) and zero current switching (ZCS) can be achieved for inner switches (T2 and T3) even at relatively low switching frequencies (4 kHz), as shown in Fig. 5. However, it can only be reached for a certain regulation range. Decreasing input voltage results in an increasing duty cycle at rated load conditions. ZCS is only

possible up to the input voltage value of 3100 V. In the case of input voltages below 3100V in the range where the duty cycle reaches its maximum, only ZVS could be reached, as shown in Fig. 5 (b). It should be noted here that during the whole input voltage range the outer switches T1 and T4 are hard switched, as shown in Fig. 6. There are several possibilities to increase the input voltage range for ZVS and even achieve ZVS for outer switches as described in [8], [9], [10]. However, these methods always require some additional components, which can be a problem in case of high voltage and high power applications.

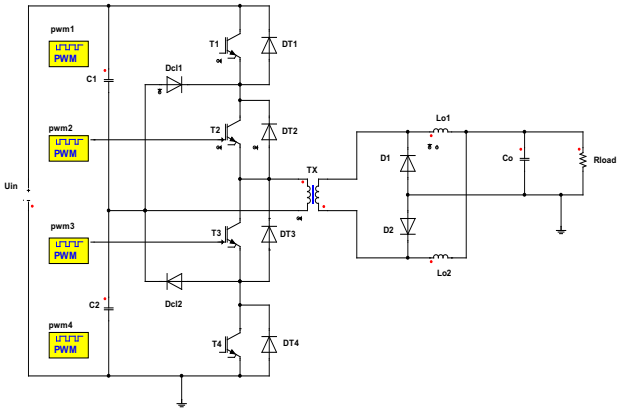
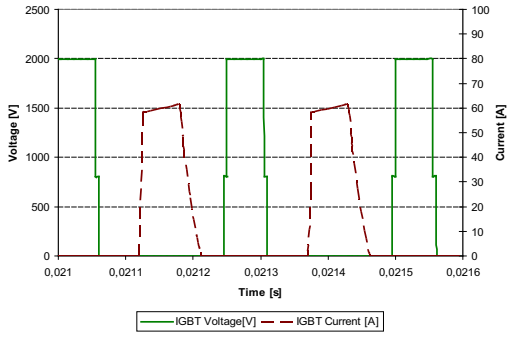
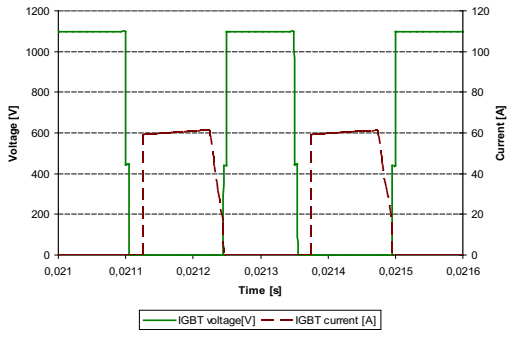


Fig. 4. Simulation circuit of the three-level half-bridge DC/DC converter with current doubler rectifier.



(a)



(b)

Fig. 5. Soft switching of inner switches T2 and T3: maximal input voltage - ZVS and ZCS (a), minimal input voltage - ZVS (b).

(a)

(b)

Fig. 6. Hard switching of outer switches T1, T4: maximal input voltage (a), minimal input voltage (b).

By the simulations it was predicted that with the proposed PWM control scheme the following benefits could be achieved:

- only two microcontroller PWM channels are required;
- ZVS is achieved for inner switches T2 and T3;
- flying capacitor is not needed, thus space-weight constraints are fulfilled.

However, several drawbacks should also be noted:

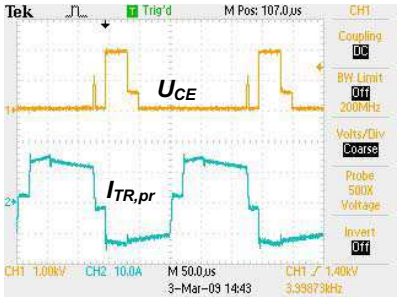
- no soft switching for outer switches T1 and T4 is achieved;
- ZCS for inner switches T2 and T3 is achievable within the limited regulation range.

B. Experimental Results

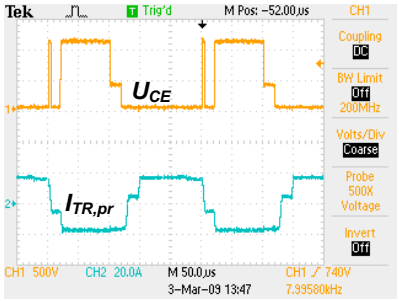
Figs. 7 and 8 show test results of the three-level half-bridge inverter. Several circumstances prevented the measurements of collector current of the inner transistors separately. Instead of that, the transformer primary current was measured, which in principle has the similar waveform. In accordance with the current shape (Fig. 7), the leakage inductance of the transformer primary winding was noticeably higher than in the simulations.

The main reason of the increased leakage inductance of the primary winding was the high voltage wiring between the inverter and transformer that add more than 15 μH to the circuit. Thus, no ZCS for the inner switches is possible in the

current case. However, ZVS is achieved over the full regulation range of the converter, as was predicted in simulations. The outer switches are constantly operating in the hard switching mode, as shown in Fig. 8.

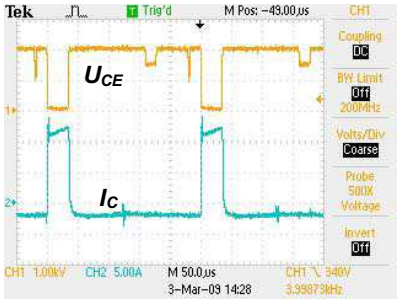


(a)

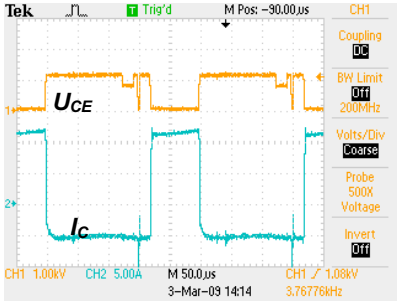


(b)

Fig. 7. Collector-emitter voltage of the inner IGBT T2 and transformer primary current: duty cycle 0.22, input voltage 3800 V (a), duty cycle 0.4, input voltage 2200 V (b).



(a)



(b)

Fig. 8. Collector-emitter voltage and collector current of the outer IGBT T1: duty cycle 0.22, input voltage 3800 V (a), duty cycle 0.4, input voltage 2200 V (b).

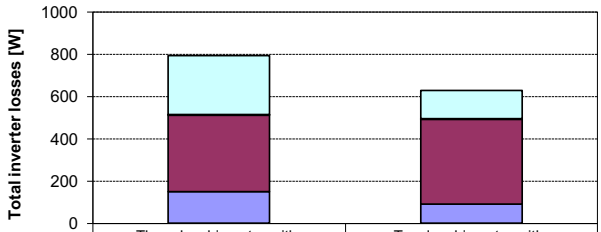
PERFORMANCE EVALUATION OF THE NEW CONVERTER

In this section the performance and efficiency evaluation of the proposed three-level half-bridge DC/DC converter with current doubler rectifier will be discussed. The evaluation results will be compared with those of two-level half-bridge DC/DC converter with full bridge rectifier, discussed in [1]. The concurrent converters will be compared for the same operation points.

A. Inverter Performance

In Fig. 9 the total inverter losses of the investigated 50 kW inverter topologies are compared with that of different high-voltage IGBTs. The inverters were evaluated at the nominal operating voltage and rated power. The switching frequencies were selected as 1 kHz and 4 kHz for the two-level and three-level topologies, respectively.

It was found, that the 3.3 kV IGBTs in the three-level configuration are dissipating 23% more heat as compared to the two-level inverter. Such high-frequency operation that produces extra losses is available for the 3.3 kV IGBTs mostly due to the better thermal handling capability than of 6.5 kV IGBTs.



	Three-level inverter with FF200R33KF2C (Uce=1800V, Ic=27.7A, fsw=4 kHz)	Two-level inverter with FZ200R65KF1(Uce=3600V, Ic=27.7A, fsw=1 kHz)
Pdyn,FWD [W]	279,0	133,6
Pstat,FWD [W]	0,9	0,6
Pdyn,IGBT [W]	366,3	406,6
Pstat,IGBT [W]	149,6	90,0

Fig. 9. Comparison of total losses of two- and three-level inverters operating at nominal input voltage and rated power.

Further analysis of the total inverter power dissipation shows that a specific drawback of the three-level inverter is the conduction losses increased by 40% due to series connection of two transistors (sum of voltage drops) during the conduction period. However, it cannot affect the overall feasibility of this topology in any load conditions. There is some minor power dissipation from clamping diodes Dcl1 and Dcl2 during the positive and negative freewheeling modes, respectively. The dissipated power mostly depends on the leakage inductance of the primary winding and the properties of the diodes implemented. For instance, with the fast recovery epitaxial diodes (FRED) and primary leakage inductance of the isolation transformer used in the project $L_{L,pr} \sim 20$ uH, the worst case power dissipation of clamping diodes was only 20 W.

B. Performance of Transformer-Rectifier Stage

The fourfold increase in the switching frequency, available from the 3.3 kV IGBTs in comparison with 6.5 kV IGBT based counterpart has a positive influence on the isolation transformer dimensions and weight, reducing the magnetic core volume by 34% for the same transferred power [11]. The twofold reduction of the number of primary turns caused by the higher operating frequency of a three-level inverter with CDR in row with the secondary current twice decreased gives an additional benefit in terms of 92 W smaller power dissipation of the isolation transformer in all operating points.

Due to the number of rectifying diodes reduced twice, in each conduction period the CDR features smaller power dissipation for the same load conditions. It should be noted that because of the doubled amplitude voltage value of the secondary winding of the CDR topology, the rectifying diodes with proportionally increased blocking voltage must be used. In the application discussed it was considered to implement the fast recovery epitaxial diodes (FRED) packaged in SOT-227B modules due to the soft recovery and almost negligible switching losses. In dual modules the diodes were connected in parallel, thus the resulting number of diodes was doubled for both topologies. The blocking voltages selected were 1.2 kV and 1.8 kV for the FBR and CDR topologies, respectively. Although the forward voltage drop for the 1.8 kV diodes was 47% higher, the resulting power dissipation of the CDR at rated load conditions was reduced by 27% in comparison with the FBR topology (610 W and 840 W, respectively).

Another source of power dissipation in the output stage of the converter is the output inductor. In FBR topology inductor handles all the output current, while in the CDR the output current is proportionally split between two output inductors. The value of the inductance required for CDR design is L_{O1}=L_{O2}= 4 mH. For the same operating conditions and output ripple limitation, the inductance considered for the FBR topology was about the same (L_O=4.8 mH). Because each inductor in the CDR topology is carrying half the output current, the total magnetic core volume in the CDR is 50% smaller than that of a single inductor in the FBR topology. The total power dissipation of two inductors in the CDR topology will be 24% less than that of the single inductor in the FBR topology (580 W and 770 W).

Finally, it should be stated that the estimated efficiency of the power stage of the new proposed converter increased about 1…1.2% as compared to its predecessor.

CONCLUSIONS

This paper has presented the analysis and design of three-level half-bridge isolated DC/DC converter aimed for the high-voltage (≥2 kV) and high-power (≥10 kW) applications. Three-level topology provides a possibility of transistor implementation with the blocking voltage twice reduced in comparison with conventional two-level configuration, that being especially topical in converters with high voltage transistors. For the same transferred power the IGBTs in the three-level configuration could be operated with at least two times higher switching frequency than in the two-level one.

Thanks to increased switching frequency and current doubler rectifier implemented in the proposed converter the power dissipation of the isolation transformer was reduced by 30%. Moreover, the 27% and 24% reductions in rectifier and inductor losses respectively, lead to approximately 1…1.2% efficiency rise of the proposed converter in comparison with its predecessor.

ACKNOWLEDGEMENT

Authors thank Estonian Science Foundation (Grant ETF7425 "Research of Dynamic Performance of High-Voltage IGBTs" and Grant ETF8020 "Research of Advanced Control and Diagnostics Systems for the High-Power IGBT Converters") for financial support of this study.

REFERENCES

[1] Jalakas, T.; Vinnikov, D.; Laugis, J., "Development of 50-kW Isolated DC/DC Converter with High-Voltage IGBTs", Compatibility in Power Electronics, 2007. CPE '07, pp.1-6, May 29-June 1, 2007.

[2] Haroen, Y.; Dahono, P.A.; Sutanto, J., "A new type of DC-DC converter for rolling stock auxiliary power supply", Proceedings of 1998 International Conference on Power Electronic Drives and Energy Systems for Industrial Growth, 1998., vol. 1, no., pp. 436-440, vol.1, 1-3 Dec. 1998.

[3] Xinbo Ruan; Bin Li; Qianhong Chen, "Three-level converters-a new approach for high voltage and high power DC-to-DC conversion", 2002 IEEE 33rd Annual Power Electronics Specialists Conference, 2002. PESC'02, vol.2, pp. 663-668, 2002.

[4] Byeong-Mun Song; McDowell, R.; Bushnell, A.; Ennis, J., "A three-level DC-DC converter with wide-input voltage operations for ship-electric-power-distribution systems", IEEE Transactions on Plasma Science, vol. 32, no.5, pp. 1856-1863, Oct. 2004.

[5] Canales, F.; Barbosa, P.; Lee, F.C., "A zero-voltage and zero-current switching three-level DC/DC converter", IEEE Transactions on Power Electronics, vol. 17, no. 6, pp. 898-904, Nov. 2002.

[6] Alou, P.; Oliver, J.A.; Garcia, O.; Prieto, R.; Cobos, J.A., "Comparison of current doubler rectifier and center tapped rectifier for low voltage applications", Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC '06, vol., pp. 7, 19-23 March 2006.

[7] Lin, B.-R.; Huang, K.; Wang, D., "Analysis and implementation of full-bridge converter with current doubler rectifier", IEEE Proceedings of Electric Power Applications, vol.152, no.5, pp. 1193-1202, 9 Sept. 2005.

[8] Jang, Y., Jovanovic, M. M.: "A new three-level soft-switched converter", IEEE Transactions on Power Electronics, Vol. 20, Jan. 2005, pp.: 75 – 81.

[9] Xinbo Ruan, Linquan Zhou, Yangguang Yan: "A Novel Zero-Voltage and Zero-Current-Switching PWM Three-Level Converter", IEEE 32nd Annual Power Electronics Specialists Conference, PESC'2001, Vol. 2, June 2001, Pp.: 1075 – 1079.

[10] Pinheiro, J.R., Barbi, I.: "Wide load range three-level ZVS-PWM DC-to-DC converter", 24th Annual IEEE Power Electronics Specialists Conference, PESC '93, June 1993, pp.: 171 – 177.

[11] Vinnikov, D., Laugis, J.: "An Improved High-Voltage IGBT-Based Half-Bridge Converter for Railway Applications", 4th International Conference and Exhibition on Ecological Vehicles and Renewable Energies EVER'2009. March 26-29, 2009, Monaco, pp. 1-6.