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Current Fed Step-up DC/DC Converter for Fuel Cell Inverter Applications

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***Abstract* - In order to use hydrogen fuel cells in domestic applications either as main power supply or backup source, their low DC output voltage has to be matched to the level and frequency of the utility grid AC voltage. Such power converter systems usually consist of a DC-DC converter and a DC-AC inverter. Comparison of different current fed step-up DC/DC converters is done in this paper and a double inductor step-up push-pull converter investigated, presenting simulation and experimental results. The converter is elaborated for 1200 W power to match the rated power of the proton exchange membrane (PEM) fuel cell located in hydrogen fuel cell research laboratory of Riga Technical University.**

I. INTRODUCTION

The research of renewable energy resources, as well as the hydrogen energy has gained a growing interest in the recent years. The hydrogen fuel cells are fully ecological, taking into account that heat and water are the only by-products, which are excreted into the environment. The typical applications of hydrogen fuel cells include electrical transport, combined heat and power generations, and even portable electronics, like mobile phones and laptop computers [1]. In order to utilize the electrical energy, produced by fuel cells, characterized by slow dynamic response, low output voltage and large voltage variations, static power converters are researched widely throughout the world.

The fuel cells used in domestic application, either as main power supply or backup source, need to be connected to the grid. Thereby their low DC voltage has to be transformed by means of a power converter into AC voltage in accordance with the grid voltage parameters. Such power converter systems usually consist of a DC-DC converter and a DC-AC converter. Because of comparatively high input and output voltage difference, most frequently as the optimal solution converters with high frequency transformer are acknowledged for the DC-DC stage [1]-[4]. There are several classic step-up converter topologies, which ensure the necessary level of output high voltage. They can be divided into two groups – voltage source converters and current fed converters. In this paper only current fed topologies are analyzed, since they are characterized by low input current ripple, which can negatively impact operation of proton exchange membrane fuel cells module [3],[4].

Comparison of different current fed step-up DC/DC converters is done in this paper and a double inductor boost push-pull converter investigated, presenting simulation and experimental results. The converter is elaborated for 1200 W power, since such is the rated power of the proton exchange membrane (PEM) fuel cell in hydrogen fuel cell research laboratory of Riga Technical University.

II. EVALUATION OF THE RELATIVE LOSSES

There are many transformer isolated dc-dc converter topologies, which could be suitable to perform the necessary voltage boost from the fuel cell voltage level to the inverter dc link voltage. Such converters are the full-bridge, half-bridge, the flyback, the forward and the push-pull basic topologies, as well as a number of their derived topologies [5], [6]. Considering the necessity of high voltage boosting function with low input current ripple, the most appropriate converters seem to be the current fed full-bridge and push-pull configurations. In the paper the full-bridge (FB) and two versions of the push-pull converter - the single inductor push-pull (SIC) and the double inductor push-pull converters (DIC) are analyzed (Fig.1.).

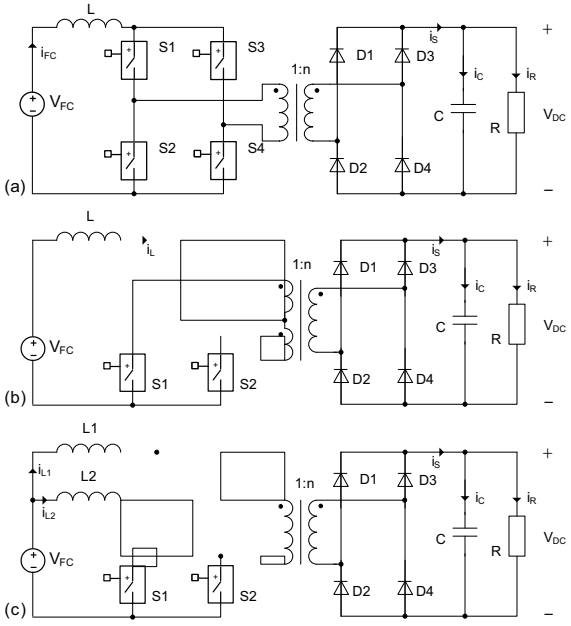

Fig. 1. Current fed converters compared: full-bridge (FB) converter; single inductor push-pull (SIC) converter; double inductor push-pull (DIC)converter.

The three topologies are compared from the viewpoint of their efficiency, calculating their relative losses in per-unit terms in respect to the FB topology.

The operation conditions considered in the comparison are summarized in Table I. The estimated converter losses are given in Table II, presenting relative losses in the switches and transformer for each topology in per unit terms. The main ratings of the analyzed converters are summarized in Table III.

TABLE I
THE OPERATING CONDITIONS OF THE CONVERTERS

Rated power	P = 1200W
Input (fuel cell)voltage	V_{FC} = 26V
Output voltage	V_{DC} = 400V
Transformer turns ratio	n = 3
Input current ripple	ΔI_{FC} = 5%
Switching frequency	f_S = 25kHz

TABLE II
RELATIVE LOSSES OF CONSIDERED CONVERTER TOPOLOGIES

Loss types	FB	SIC	DIC
P_{SW}, switch (switching loss)	1	1	0.5
P_C, switch (conduction loss)	1	0.5	0.56
P_{COPPER}, transf	1	1	0.5
P_{CORE}, transf	1	1	1
P_{COPPER}, inductor	1	1	0.64

The presented analysis is used as a guide to choose the topology that is the most attractive concerning the efficiency of the converter. The values introduced in Table II are mostly a rough guide, since this classification was made based on a simplified circuit analysis.

The following assumptions were made during comparative analysis:

- V_P, f_S, t_r+t_f, R_{on}, I_{FC} and ΔI_{FC} are identical for all the three cases;
- All the three converters have identical cores in the boost inductors and transformers respectively.

The equations used to compare the three current fed converter topologies are summarized in Table IV.

From the above analysis it can be seen that the core losses in the transformer are the same for all three configurations. The losses in switches are considerably lower for the DIC topology. This is an important advantage since the largest losses in the considered converters appear in the switches and reducing them considerably improves the converter efficiency. The transformer losses also appear to be the smallest for the DIC among the considered topologies.

TABLE III
THE MAIN RATINGS OF THE CONSIDERED CONVERTERS

Parameter	FB	SIC	DIC
Number of switches	4	2	2
Number of Boost Inductor	1	1	2
Transformer	1 primary winding	2 primary windings	1 primary winding
Switch peak voltage	V_{DC}/n	$2\cdot V_{DC}/n$	V_{DC}/n
Switch rms current (I_{SW_rms})	$I_{FC}\sqrt{2-D}/2$	$I_{FC}\sqrt{2-D}/2$	$I_{FC}\sqrt{2-D}/2$
Boost inductors current	I_{FC}	I_{FC}	$I_{FC}/2$
Inductor current ripple frequency	$2\cdot f_S$	$2\cdot f_S$	f_S
Trafo peak volt- ampere	$(V_{DC}/n)\cdot I_{FC}$	$(V_{DC}/n)\cdot I_{FC}$	$(V_{DC}/n)\cdot I_{FC}/2$
Duty-cycle (D)	$D=1-\frac{V_{FC}\cdot n}{V_{dc}}$	$D=1-\frac{V_{FC}\cdot n}{V_{dc}}$	$D=1-\frac{V_{FC}\cdot 2n}{V_{dc}}$

TABLE IV
THE EQUATIONS USED IN THE EFFICIENCY COMPARISON OF FB, SIC AND DIC CONVERTER TOPOLOGIES

	FB	SIC	DIC
P_{SW}, switch	$4\left(\frac{I_{FC}}{2}\right)V_P f_S(t_r+t_f)$	$2\left(\frac{I_{FC}}{2}\right)2V_P f_S(t_r+t_f)$	$2\left(\frac{I_{FC}}{2}\right)V_P f_S(t_r+t_f)$
P_C, switch	$4\cdot I_{SW\_rms}^2\cdot R_{on}$	$2\cdot I_{SW\_rms}^2\cdot R_{on}$	$2\cdot I_{SW\_rms}^2\cdot R_{on}$
P_{COPPER}, transformer	$R_P(1-D)I_{FC}^2+R_S(1-D)\frac{I_{FC}^2}{n^2}$	$R_P(1-D)I_{FC}^2+R_S(1-D)\frac{I_{FC}^2}{n^2}$	$R_P(1-D)\left(\frac{I_{FC}}{2}\right)^2+R_S(1-D)\left(\frac{I_{FC}}{2\cdot n}\right)^2$
P_{CORE}, transformer	$K\cdot f_S^{m1}\cdot B^{m2}\cdot W_{tFe}\cdot 10^{-3}$	$K\cdot f_S^{m1}\cdot B^{m2}\cdot W_{tFe}\cdot 10^{-3}$	$K\cdot f_S^{m1}\cdot B^{m2}\cdot W_{tFe}\cdot 10^{-3}$
L inductor	$L=\frac{D\cdot V_{FC}}{2\cdot\Delta I_{FC}\cdot 2\cdot f_S}=\frac{N^2}{\Re}$	$L=\frac{D\cdot V_{FC}}{2\cdot\Delta I_{FC}\cdot 2\cdot f_S}=\frac{N^2}{\Re}$	$L=\frac{D\cdot V_{FC}}{2\cdot\Delta I_{FC}\cdot f_S}=\frac{N^2}{\Re}$
P_{COPPER}, inductor	$I_{Lrms}^2\cdot R_L=I_{FC}^2\cdot MLT\cdot N\cdot R_{spec}$	$I_{Lrms}^2\cdot R_L=I_{FC}^2\cdot MLT\cdot N\cdot R_{spec}$	$I_{Lrms}^2\cdot R_L=I_{FC}^2\cdot MLT\cdot N\cdot R_{spec}$

where: V_p is the primary voltage of the transformer, R_{on} - the on-state resistance of the switches, R_p – the resistance of the primary winding of the transformer, R_s – the resistance of the secondary winding of the transformer, I_{Lrms} - the inductor RMS current (for one inductor), R_L - the inductor series resistance, N - the number of turns for the inductor, MLT - the inductor turn mean length, R_{spec} - the specific resistance of the inductor wire (μΩ/cm) and $\Re$ is the core magnetic reluctance (considered to be the same for all the three converters).

Due to the double number of inductors (with larger inductances), the inductor losses will be the largest for the DIC topology. However, taking in account that the inductor losses have relatively low contribution to the total losses, the above comparison suggests that the most promising topology is the DIC push-pull converter. Thereby this converter has been chosen to be designed and realized in simulation and experimental stages. Two input chokes expected larger DC/DC converter dimension, but at the same time they serve as input filter.

III. DESIGN OF THE DIC STEP-UP CONVERTER

Since there is relatively low voltage and high current at the primary side, both the inductors and the switches must be able to handle this high current, which, even at low on-resistance will cause significant conduction losses in the components.

These losses can be decreased in two basic ways: by decreasing the resistance of the components and by reducing the current, which flows through them. Reduction of the current can be achieved by connecting two or more identical converters in parallel. At parallel topology of two converters the current load on the switches will be halved and the overall switch conduction losses will halve as well, despite that the number of elements will be double.

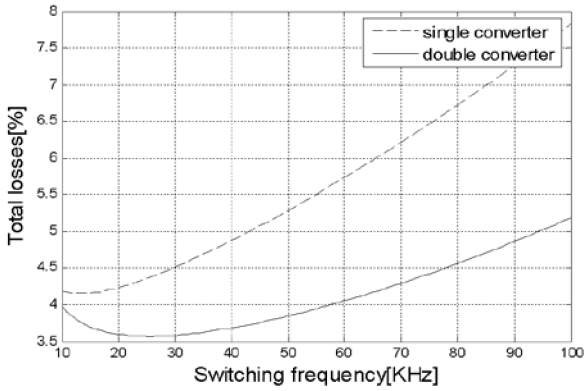

Fig. 2. Converter losses as a function of switching frequency

As the above figures show, the double converter topology has a higher efficiency than just a single converter, mainly due to halving the conduction losses in the switches. It can be seen from Fig. 2 that the most important losses are those in the switches; thereby halving them can substantially increase the overall efficiency of the converter.

The losses vary in function of the switching frequency. Fig.2. shows that the minimum losses appear between 15 and 25 KHz. It was decided to use the highest frequency from this range 25 kHz in order to minimize the needed inductance.

A. Protection of the Switches and Overvoltage clamping

The hard switching converters have a drawback of voltage overshoots at turn-off due to the energy stored in the parasitic inductances. These voltage spikes are not only dangerous to the transistors but they substantially increase the switching losses.

There are two basic ways to protect the transistor switches from being damaged by the overvoltage. The first is using transistors with blocking voltage ratings that exceed these stresses. This, however, results in poor utilization of the transistors, since on state resistance of the MOSFET transistors increases dramatically with increased blocking voltage. The other way is to limit the stresses within safe levels using snubber circuits. The highest voltage spikes across the switches in the topology under consideration appear at turn-off, when the overvoltage occurs due to the transformer leakage inductance. Therefore a passive clamping circuit together with conventional RC snubber circuits were implemented to limit the voltage during turn-off (see Fig.3), [5].

IV. SIMULATION OF THE DIC CONVERTER

The simulation of the DIC converter was done using LTspice simulation tool. Since a steady operation point was to be examined, the FC was modeled by a constant voltage source. The core losses of the inductances were neglected. The transformer was modeled as an ideal transformer introducing the leakage inductance in series. The switches (MOSFET transistors – IXFN73N30) were modeled using SPICE models provided by the manufacturers. The control circuit was realized using programmable voltage sources.

Fig. 3. shows the schematics of DIC converter with passive clamping in LTspice environment. The operation conditions of the simulation are adjusted to the rated parameters of the converter given in Table I. Active load with a small filter capacitor of 10μF was considered.

The capacitor of the clamp circuit has to ensure that the clamp circuit overtakes the energy from the transformer leakage inductance, without increasing voltage of the switches beyond safe values and can be calculated from the following equation:

$$C_{clamp} = \frac{2 \cdot L_{lk} \left(I_{FC} + \Delta I_{FC} \right)^2}{V_{clamp}^2 - V_{norm}^2}, \quad (1)$$

where: C_{clamp} is the capacitance of the clamp capacitor, L_{lk} is the leakage inductance of the transformer, U_{clamp} is the maximum, but U_{norm} – normal voltage of the clamp capacitor.

The clamp resistor, on the other hand, has to be calculated to discharge the clamp capacitor to its normal voltage and dissipate the energy collected from the leakage inductance, according to:

$$R_C = \frac{\left(V_{norm} - V_{FC} \right)^2}{P_{lk}}, \quad (2)$$

where

$$P_{lk} = \frac{1}{2} \cdot L_{lk} \cdot \left(\frac{I_{FC} + \Delta I_{FC}}{2} \right)^2 \cdot 2 f_S, \quad (3)$$

is the power to be dissipated in the clamp resistor.

Unfortunately such passive clamping circuit can be optimized for only one operation point, so the maximum load condition was chosen for calculation, since it is the worst case. The value of leakage inductance (L_{leak} = 4μH) was obtained experimentally, by measuring the transformers mutual and self-inductances.

Simulation waveforms of a steady state operation are shown in Fig.4. From waveforms it is evident that the transistor voltage does not exceed the maximum allowed voltage of transistor 300V. Also the transistor current is well within the allowable limits (less than 73A).

It can also be noted, that the converter operates as desired, providing 400 V output voltage at rated input and load conditions.

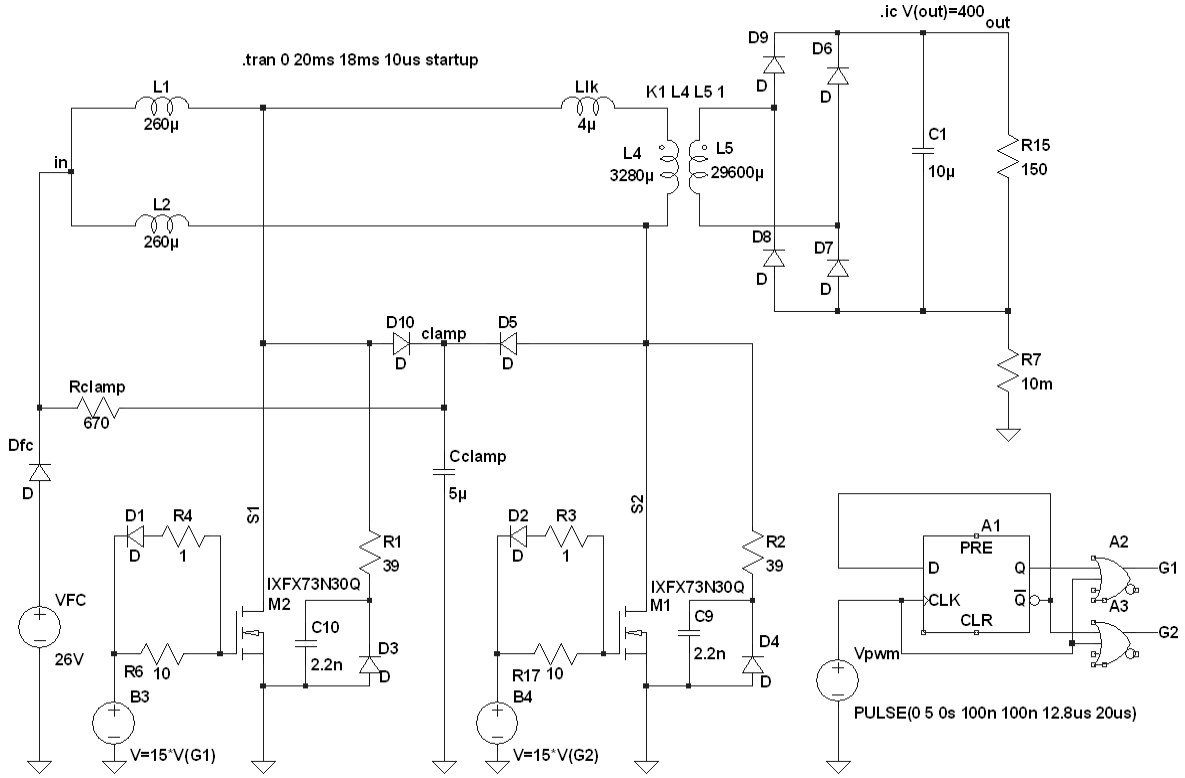

Fig. 3. DIC converter with passive clamp circuit in LTspice environment

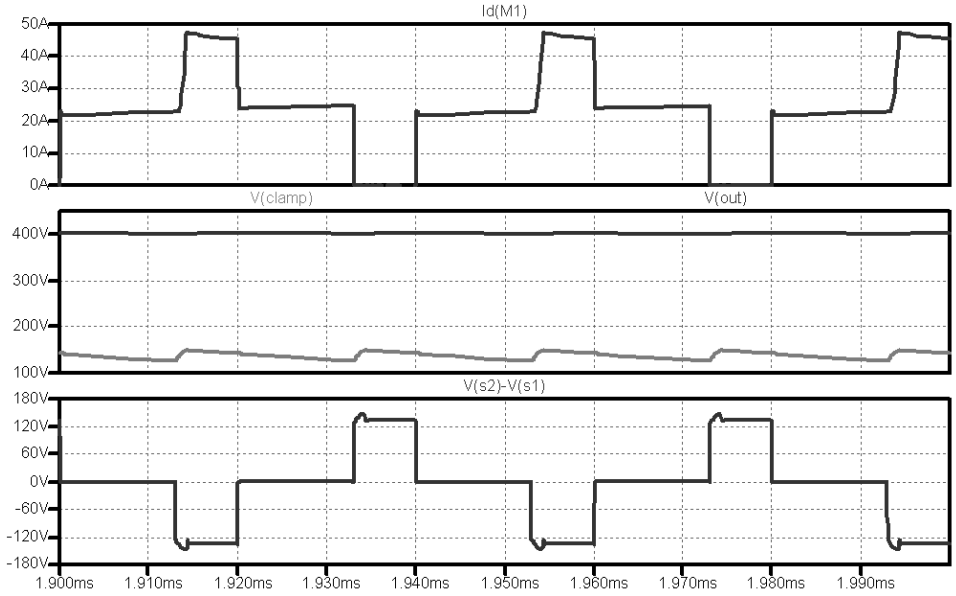

Fig. 4. Simulated waveforms of the DIC converter: from the top – current through transistor M1, output voltage, voltage of the clamp capacitor, transformer primary voltage.

V. EXPERIMENTAL TESTS

Experimental testing of one DIC converter was carried out as well. The testing was performed using two 12V 50Ah car batteries in series as the input voltage source and connecting the DIC converter to a resistive load. Measurements of the input current, transformer input voltage and load voltage and current were done. Then the efficiency of the converter was calculated.

The first version of the prototype is shown on Fig.5. After preliminary testing it was decided to optimize the snubber circuits and the layout of the board by placing the transformer closer to the power switches and thus decreasing additional leakage inductance in the path of primary current. The converter with the optimized board layout is shown in Fig.6.

The clamping resistor was chosen 670Ω and clamping capacitor 5,69 μF. In case the resistor is too small and the clamping capacitor discharges too fast, there is the possibility to decrease the voltage on the clamping capacitor below the transformer primary voltage, causing the clamping diodes to work as a rectifier of the primary voltage which reduces the overall efficiency of the converter. In parallel with the power transistors, RC snubber circuits were implemented composed of 2,2 nF polyester film capacitors and 39Ω 5W resistors.

The results of experimental testing are summarized in Table V. The tests were performed below the rated power of the converter (approximately 750W at the output), because the turn-off voltage overshoots across the transistor switches were dangerous to transistors when approaching full load conditions.

TABLE V
THE MEASURED QUANTITIES

Parameter (average values)	Measurement	
	First layout	Optimized layout
Vin	23.3 V	23.6 V
Vout	411 V	410 V
Iin	35.8 A	34.7 A
Iout	1.78 A	1.82 A
efficiency	0.88	0.91

The estimated efficiency of the DIC converter with the optimized board layout was 91%. Connecting two DC/DC converters in parallel would slightly increase the overall efficiency, as mentioned in chapter III. Anyhow, in order to increase the efficiency considerably, an active clamp circuit needs to be applied, avoiding the loss of the energy stored in the leakage inductance.

Experimental waveforms of the DIC converter both - with the first and the optimized board layouts are shown in Fig.7. and Fig.8. respectively. As evident from the waveforms, the drain to source voltage across the transistor has improved due to the optimized board layout and improved snubber circuitry. Nevertheless, at full load conditions the turn-off voltage overshoots are close to the maximum transistor blocking voltage (300V) signifying that further optimization of the clam and snubber circuits needs to be carried out.

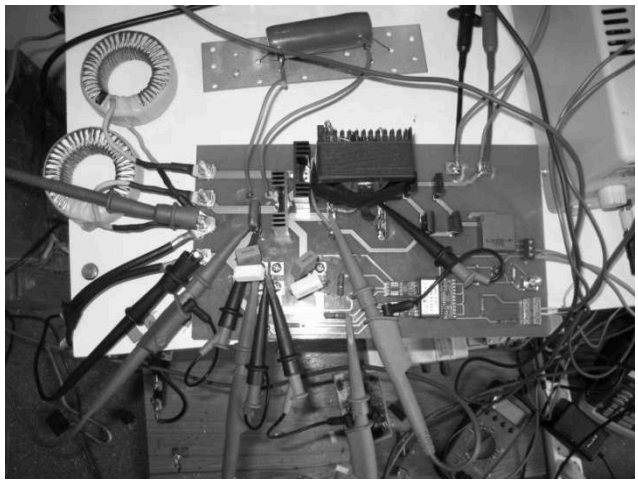

Fig 5. The first version of the experimental prototype of DIC converter

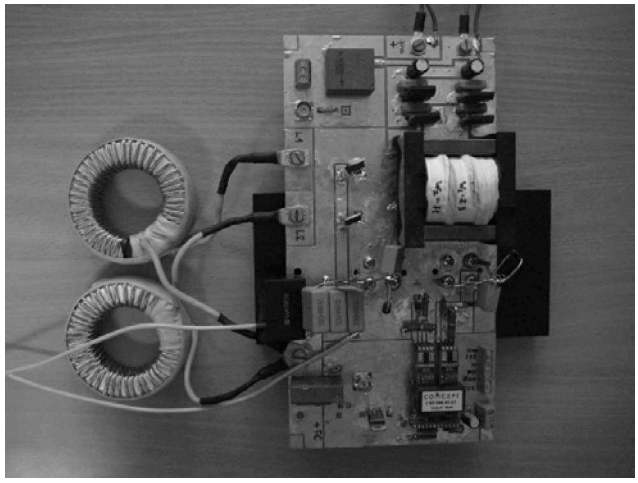

Fig 6. The optimized version of board layout of the DIC converter

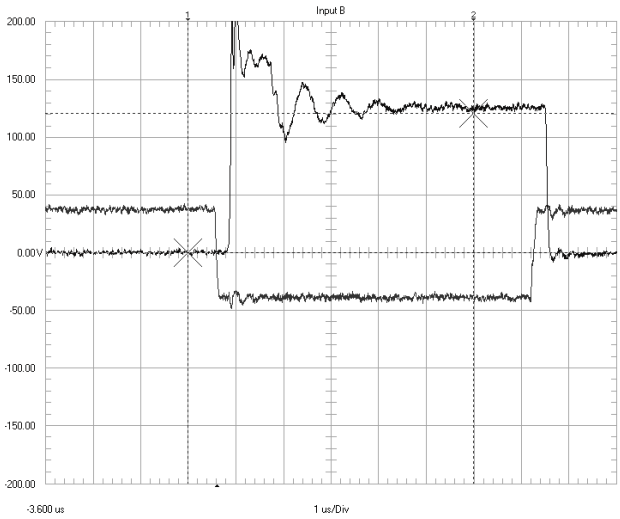

Fig.7.Experimental waveforms of the DIC converter with the first board layout – from the top: control voltage, voltage across one power transistor.

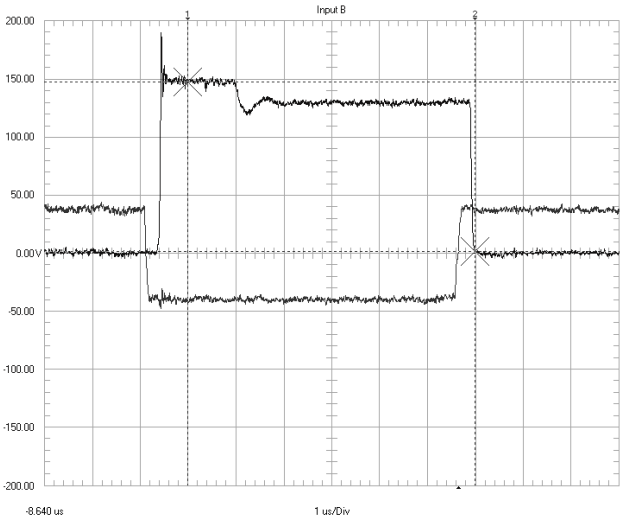

Fig.8.Experimental waveforms of the DIC converter with the optimized board layout – from the top: control voltage, voltage across one power transistor.

The input current and voltage of the optimized prototype are shown on Fig.9. As evident, the input current ripple is ± 1,5A (less than 5% of the average value of the current), which is satisfactory.

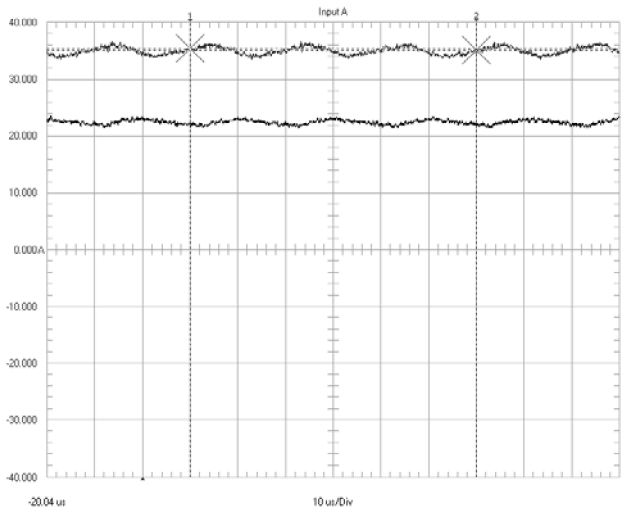

Fig.9.Experimental waveforms of the DIC converter with the optimized board layout – from the top: input current, input voltage.

VI. CONCLUSIONS

Fuel cell as electrical energy generation system provides a lot of benefits - the system has high efficiency, very low noise level and imposes no environmental pollution.

In applications where fuel cell has to be connected to the grid, the power converter usually consists of step-up DC/DC part and a DC/AC inverter part. Considering the necessity of high voltage boosting function with low input current ripple, the most appropriate converters seem to be the current fed full-bridge and push-pull configurations. In the paper the full-bridge and two versions of the push-pull converter: the single inductor push-pull and the double inductor push-pull converters are analyzed and compared from the viewpoint of efficiency. The double inductor push-pull converter being the most efficient topology has been simulated in LTSpice environment and tested experimentally.

After preliminary experimental testing it was decided to optimize the snubber circuits and the layout of the board by placing the transformer closer to the power switches and thus decreasing additional leakage inductance in the path of primary current. It was acknowledged that the optimized board layout performs well and the efficiency of the converter is above 90%. Connecting two DC/DC converters in parallel would slightly increase the overall efficiency, nevertheless, in order to increase the efficiency considerably, an active clamp circuit needs to be applied, avoiding the loss of the energy stored in the leakage inductance. The ripple of the input current of the optimized prototype is below ± 5% of the mean value, which is within acceptable limits.

The elaborated prototype of double inductor push-pull DC/DC converter can be used as a background for further work on clamp circuit optimization and elaboration of closed loop current control systems.

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