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Voltage Monitoring on Capacitor of Modular Multilevel Converter

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***Abstract*-A modular multilevel converter is an attractive solution for power conversion without transformers. As modular multilevel converter consists of cascade connections and floating dc capacitors, it requires continuous voltage monitoring. This paper represents voltage measurement circuit of a DC-storage capacitor including power supply with results of experiments.**

I. INTRODUCTION

Multilevel converters have emerged as a very important alternative in the area of high power medium-voltage applications. Some of the characteristics that have made these power converters popular for industry and research are: transformer elimination, lower common mode voltage, voltage operation above classic semiconductor limits and near sinusoidal outputs together with a small instantaneous rate of voltage change [1]. Commonly used topologies are: Neutral Point Clamped, Flying Capacitor, Cascaded H-Bridge and other similar modifications to these [1]. New modifications of multilevel converters have been proposed and presented at international conferences and symposiums of power converters and one of these modifications is a Modular Multilevel Converter (MMC) concept [2]-[9].

The sub-module of MMC is a two terminal device composed of two switches and DC-storage capacitor as depicted by Fig. 1. The voltage of any sub-module can be controlled by software. The individual voltages of the sub-module may even be chosen unequal and this option can be used to increase the number of resulting voltage steps. In a case of defective sub-module, it can be replaced with redundant sub-module in the arm by control action without mechanical switches. This results in an increased safety and availability [5].

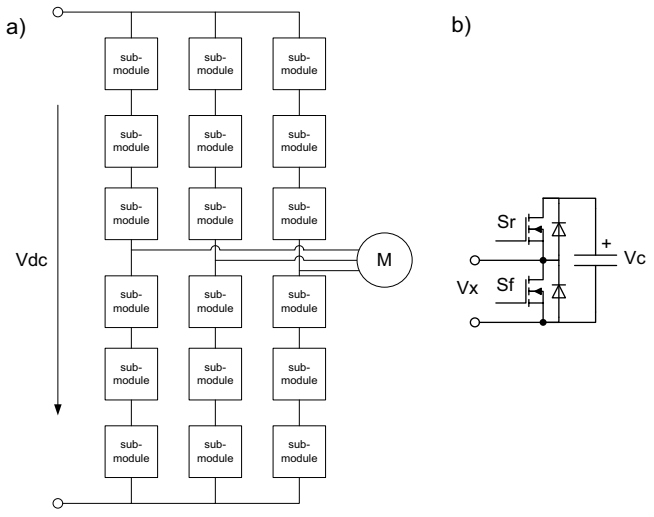

Fig. 1 Three phase Modular Multilevel Converter (a) and one sub-module (b)

Table I represents the commonly used control states of a sub-module [2]. When the switch S_F is switched on, the voltage V_X is zero. To apply the voltage V_C to the terminals, the switch S_R has to be switched on. In case of switching off both switches, the impressed voltage to the power devices is limited by the voltage V_C of capacitor.

TABLE I
COMMONLY USED SWITCH STATES OF A SUB-MODULE

Mode	SF	SR	ia	VX	dVC/dt
1	Off	On	>0	VC	>0
2	Off	On	<0	VC	<0
3	On	Off	>0	0	0
4	On	Off	<0	0	0

The voltage of the capacitor is periodically measured with a typical sampling-rate in less than the millisecond-range. According to voltages, capacitors are sorted by software. In that case of the positive current the required number of sub-modules, determined by the output state controller, with the lowest voltages is switched on and the selected capacitors are charged. When the current in the corresponding arm is negative, the demanded number of sub-modules with the highest voltages is selected. Using this method, continuous voltage balancing of the capacitors is guaranteed. This concept allows an optimized utilization of the stored energy and evenly distributed power loses for the installed electrical devices. The power losses could be kept low by switching the sub-modules solely when a change of the output state is requested.

II. VOLTAGE MEASUREMENT CIRCUIT OF A CAPACITOR

For measuring the voltage of a capacitor it was chosen to use resistors for voltage transducer and this reduced voltage convert into a signal of pulses with known frequency. Increase of the voltage across the capacitor will increase the frequency and contrariwise, decrease of the voltage – decreases the frequency. This signal is connected to an input of the FPGA board. A program in the FPGA board calculates the frequency of a signal. Detailed voltage measurement circuit is depicted by Fig. 2.

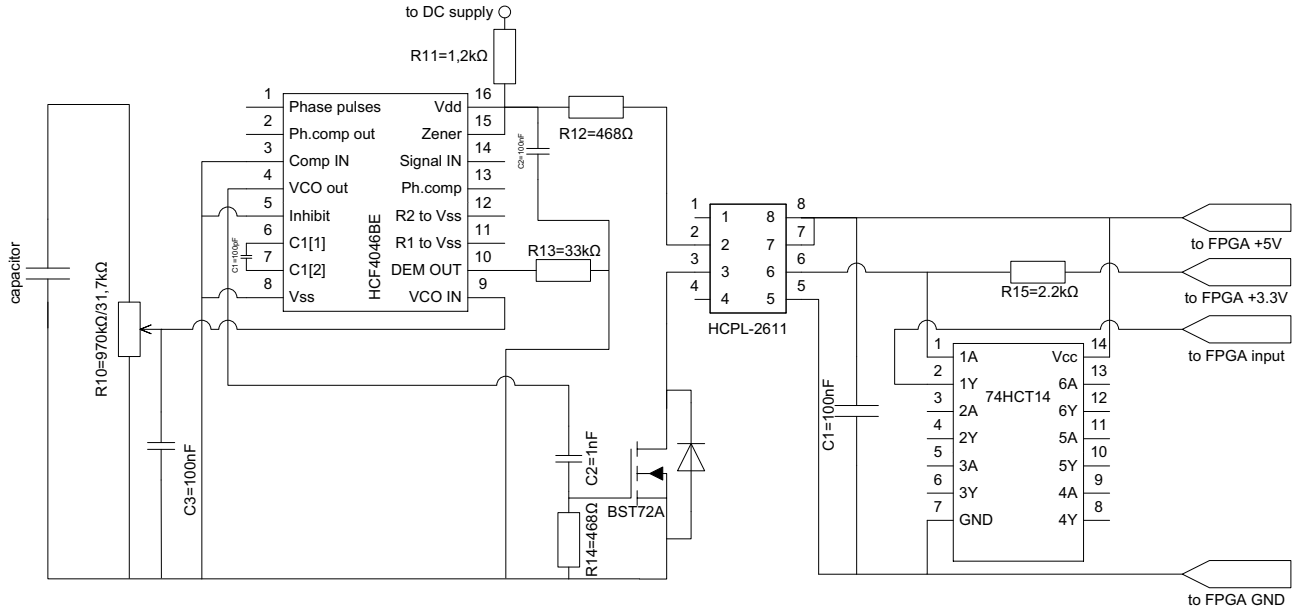

Fig. 2 Voltage measurement circuit of a capacitor including optical insulation to FPGA board

Integrated circuit (IC) HCF4046 (Fig. 2.) is being used to generate the signal of frequency depending of an input voltage at the pin 9 – the pulsed output signal is generated at the pin 4. Resistor R_{10} is being used to adjust the ratio between voltage of the capacitor and the frequency. For the capacitor's voltage 100V, the output's frequency is 100 kHz. Capacitor C_2 and resistor R_{14} are used to get a short positive pulse width – approximately 1μs.

To potentially isolate the FPGA board from the sub-module, the optocoupler (HCPL-2611) is being used with resistor R_{12} for current limitation. The transistor BST72A is being used to drive the optocoupler. Optocoupler and transistor were chosen in an experimental way.

To increase the characteristics of the output signal at the pin 6 of the optocoupler, a Schmitt trigger is being used. The rest of all inputs of a Schmitt trigger were connected to the ground. As Table II shows, signals' characteristics like falling and rising times considerably improve, for example, the rise time of the signal from 120ns to 5ns. The second output signal was inverted twice and it demonstrates that it only slow down rising and falling times of an input signal, for example, the rise time of signal from 5ns to 10ns.

TABLE II
SIGNAL CHARACTERISTICS OF TRIGGER

Signal	Rise time	Fall time
Schmitt-trigger's input	≈120ns	≈7.5ns
Schmitt-trigger's output 1	≈5ns	≈3.3ns
Schmitt-trigger's output 2	≈10ns	≈4.7ns

IC HCF4046BE was powered by energy stored in a capacitor and the predicted voltage decrease in time, if energy stored in capacitor is approximately 2000μF and current consumption is 1mA, then $du/dt=0.5V/s$.

As there was a requirement also for some auxiliary power supply for drivers of power transistors, this IC HCF4046BE was equipped with the separated power supply.

III. PROGRAMMING OF FPGA

This laboratory set of the FPGA board was used for control of MMC switches including feedback, for example, sensing a voltage on capacitors. The external FPGA board is a Xilinx Spartan3 XC3S1000-FT256 which is implemented in a Digilent Sparatan3 system board.

A freeware Xilinx ISE Design Suite10.1 Web pack from ISE foundation was used. VDHL is being used as a language for programming the FPGA board. This freeware includes everything to successfully program the FPGA board. In an experimental way, it has been discovered that there is a conflict between Xilinx ISE Design Suite10.1 and PSCAD software. ISE Simulator could not operate if the PSCAD software includes some of the FORTRAN's compilers installed at the same time.

A. The program "measure"

The program "measure" is for measuring the frequency of the input signal which comes from an external measurement circuit of a capacitor. As the measured voltage varies from 80 V up to 120 V and then the input signal value to FPGA board can be from 66 kHz up to 135 kHz.

To be sure, that program "measure" works as designed, the Digital to Analog Converter (DAC) is connected to an output of the FPGA board. There are three pins connected from the FPGA board to the DAC:

The first connected pin "chip select" (cs_n) requires an active-low signal to enable the serial clock and data functions of the DAC. The second pin is the serial clock input (sck) of the DAC. The third pin is serial data input (sdi) of the DAC.

B. The flowchart of the program

The flowchart of the program "measure" is depicted by Fig.3. This program is for sending a data to the DAC connected to an output of the FPGA board.

Primarily thing is to wait until the input signal changes its value from '1' to '0' (detects falling edge). Then start a counter and continue to count (increase counter value by 1) until next edge from '1' to '0' triggering occurs – end of one cycle or until a counter overflow occurs. It was considered to choose falling edge of signal for triggering because the signal falling time was less than the rise time (Table II). Then the counted number is being sent to the input of the DAC which is realized by "setbit", "writebit" and "shiftbit" states.

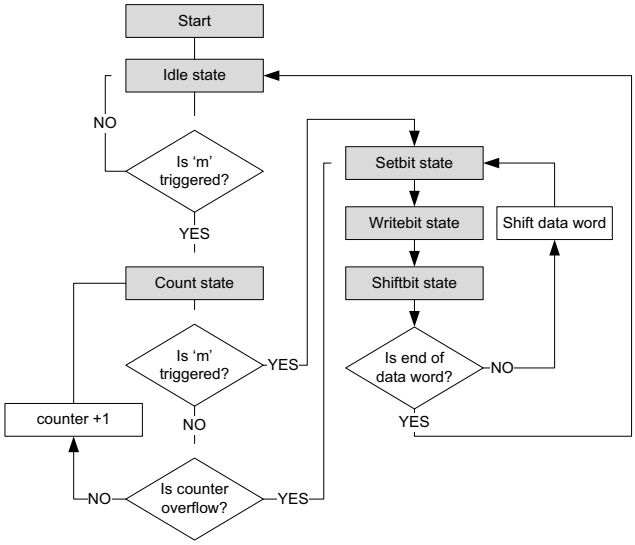

Fig. 3 Algorithm of program "measure"

IV. THE POWER CIRCUIT WITH DRIVERS OF SWITCHES

As there was available previous made circuit board (full-bridge power converter) in the laboratory, it was decided to modify it for our needs. The same or alternative components were chosen for our power converter to built-up (Fig. 4). Except that an additional power supply was needed for the driver, which controls the upper arm. So there is a need to build-it up also, described in the next chapter.

The signal to an input of a driver at the pin 2 was connected to the signal generator as there was no program still written for control in to the FPGA board.

MOSFETs were taken as switches (IRFP450). They are capable to work with current 14 amps at drain-to-source voltage 500 volts.

The driver's part number is IR21094. By the pin 3, it is possible to enable or disable the operation of the driver. The floating power supply is applied to the pin 13 and to the pin 11, and the dead time can be modified by a resistor R7 at the pin 4.

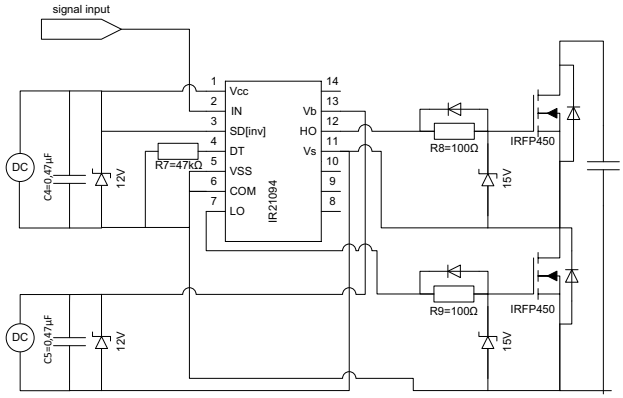

Fig. 4 Power switches with drivers

V. ADDITIONAL DC/DC POWER SUPPLY

Fig. 5 represents additional power supply for driver and measurement circuit. IC HCF4046BE also was used for frequency generation as in a measurement circuit, but in this case it controls transistors BST72A at the primary side of the transformer. A Schmitt trigger inverter is used for opposite transistor. The switching frequency is 100 kHz. Resistor R4 is for current limitation in the transformer. One secondary output of power supply is for driver and a measurement circuit, but the other one is for the floating power supply for control of upper-arm of half-bridge. The toroidal transformer with the ferrite core was used. Dimensions of core are the following: height – 6,5mm, outer diameter - 16,5mm, inner diameter – 9mm.

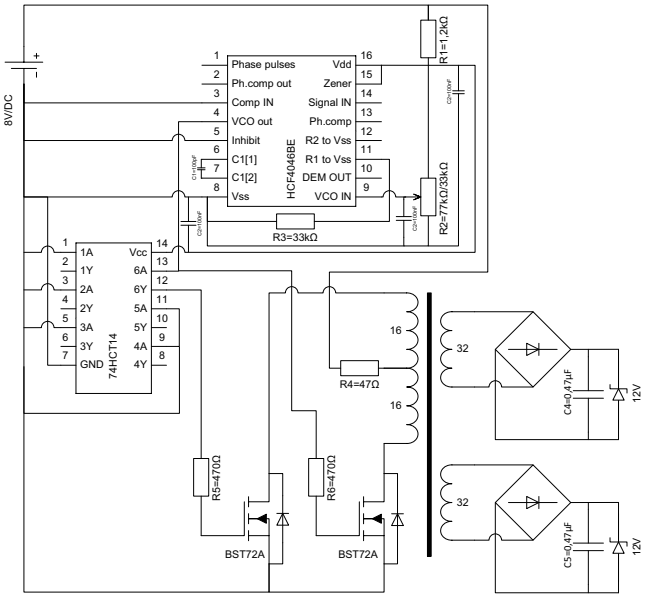

Fig. 5 Power supply for drivers and voltage measurement circuit

10 turns were wired up on the core. Signal generator was used as alternating voltage source with resistor connected in series for limitation of current. Voltage was measured on windings and on the resistor for calculations of current:

$$I=U/R \quad (1)$$

Windings' impedance was calculated by:

$$Z=U/I \quad (2)$$

and inductance by equation:

$$L=Z/\omega=Z/(2\cdot\pi\cdot f) \quad (3)$$

and inductance per turns squared:

$$l=L/\text{turns}^2. \quad (4)$$

At different frequencies inductance were calculated as shown in Table III.

TABLE III
CHARACTERISTICS OF CORE

Frequency ,kHz	U, V	I, mA	Z, Ω	L, µH	l, µH/t2
20 (sat.)	3,68	68	54	430	4,30
50	6,46	38	170	541	5,42
100	7,60	19	400	637	6,37
200	8,06	10	806	641	6,41
500	8,12	6	1476	470	4,70

As the number of turns N_1 and inductance L_1 were known, then the inductance L > 6366µH. And then the number of the turns can be calculated as:

$$n>(L/l)^{0.5}\approx 32 \text{ turns}. \quad (5)$$

At the end at the primary side were 2·16 turns and two secondary winding outputs with 32 turns per each.

VI. EXPERIMENTAL PART

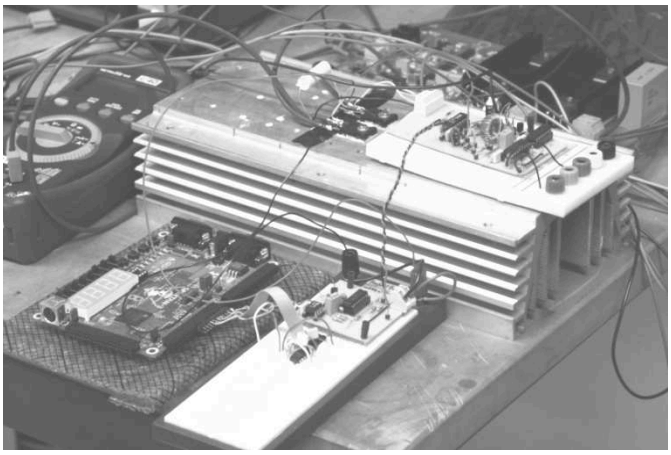

Fig. 6 Laboratory test bench of one sub-module

Fig. 6 represents laboratory test bench of a one-module which includes: power circuit with drivers, the capacitor's voltage measurement circuit, DC/DC power supply and FPGA board with DAC.

A. Voltage measurement circuit of a capacitor

If the measured capacitor's voltage is 100V, then the output signal of IC HCF4046BE is as depicted by Fig. 7. Duty cycle of an output signal is 50 percent. Capacitor between the output of HCF4046BE and the gate of transistor realize small voltage pikes between gate and ground (Fig. 7 (2)).

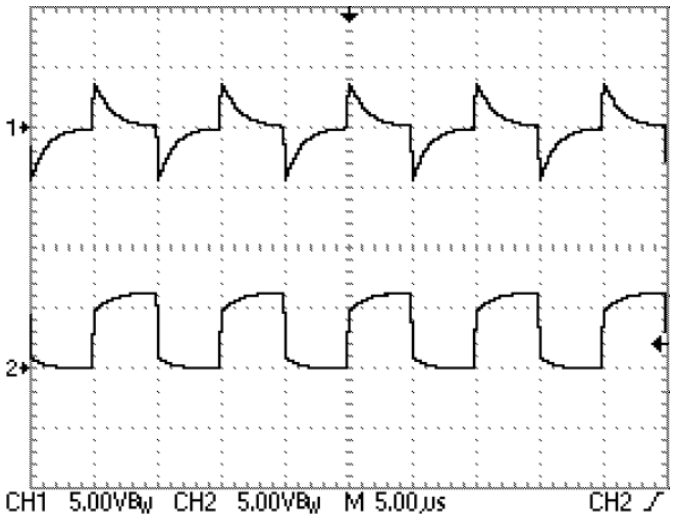

Fig. 7 Voltage of transistor's gate (1) and output signal (2) of IC

Fig. 8 represents voltage of the gate of transistor (1) and the voltage of the collector and the emitter of transistor (2) and as it approves that duty cycle is 10 percent. Less power is consumed to switch on the diode of the optocoupler than if transistor would be directly connected to an output of IC.

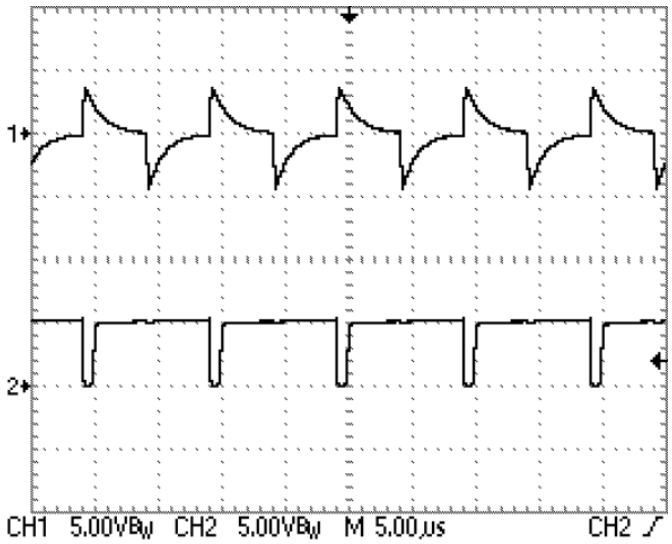

Fig. 8 Voltage of transistor's gate (1) and of transstor's collector and emitter (2)

Fig. 9 (1) depictures output signal of the optocoupler and (2) signal to the FPGA board, inverted by a Schmitt trigger. It was mentioned above that Schmitt trigger improves the f rise time of signal as it was necessary for the better counting process in to the FPGA board.

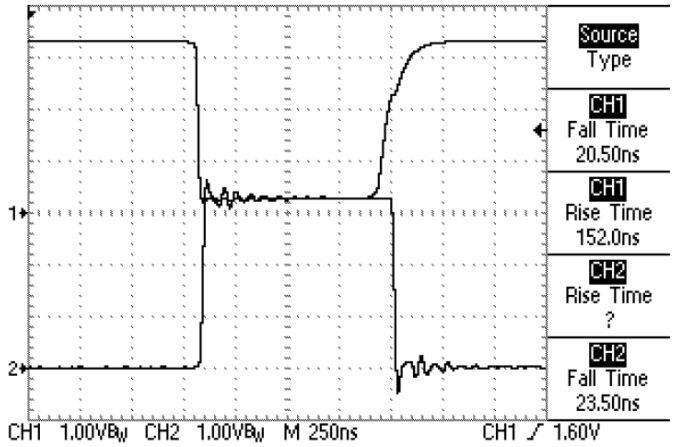

Fig. 9 Output of the optocoupler (1) and input to the FPGA board (2) expanded

Increasing the voltage of a capacitor – the frequency of the output signal also increases as it is shown in Fig. 10. The first experiment with a wrong capacitor (1nF) was soldered instead of 0,1nF (dotted line). Operation voltage range could be from 80V to 120V, so the frequency shall be from 66.1 kHz up to 135.6 kHz correspondingly.

The test of the voltage measurement circuit operating at different conditions of temperature was done. It worked as predicted, that increase of temperature – increases the frequency of the input signal. Difference in percentage between the normal condition (at 25°C) and increased temperatures is summarized by Table IV. In the case of temperature feedback in this module, predicted error could be added to the program.

TABLE IV
CHANGES OF FREQUENCY AT VARIOUS INPUT VOLTAGE AND TEMPERATURE

DC, V	≈35 °C	≈40 °C	≈50 °C	≈57 °C	≈73 °C
50	16,91%	24,67%	34,80%	40,53%	44,33%
60	8,31%	12,77%	18,49%	23,06%	26,03%
70	5,57%	7,77%	12,12%	15,03%	18,24%
80	3,78%	5,84%	8,95%	10,80%	13,71%
90	3,22%	4,54%	7,06%	9,07%	11,09%
95	2,82%	4,12%	6,34%	7,82%	10,05%
100	2,49%	3,69%	5,74%	7,20%	9,43%
105	2,30%	3,41%	5,23%	6,51%	8,53%
110	2,06%	3,25%	4,73%	5,86%	7,97%
115	2,00%	2,75%	4,29%	5,56%	7,35%
120	1,74%	2,52%	3,83%	5,11%	6,74%

B. Check if program "measure" works

To make sure that program "measure" works properly, a DAC (Digital-to-Analog Converter) was added to an output of FPGA board. Schmitt trigger was added at input of FPGA board, but it still did not fix some of the problems (Fig. 11). However characteristics of input signal were improved.

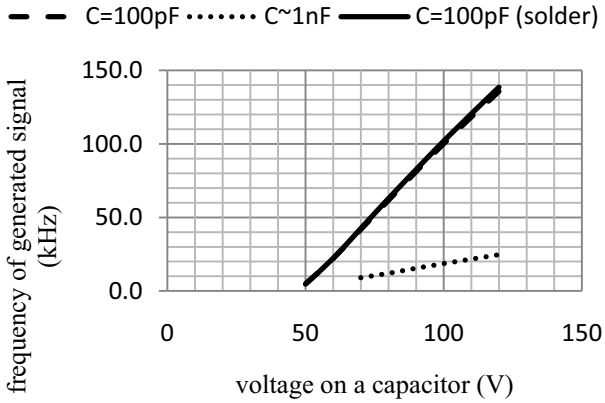

Fig. 10 Voltage vs. Frequency

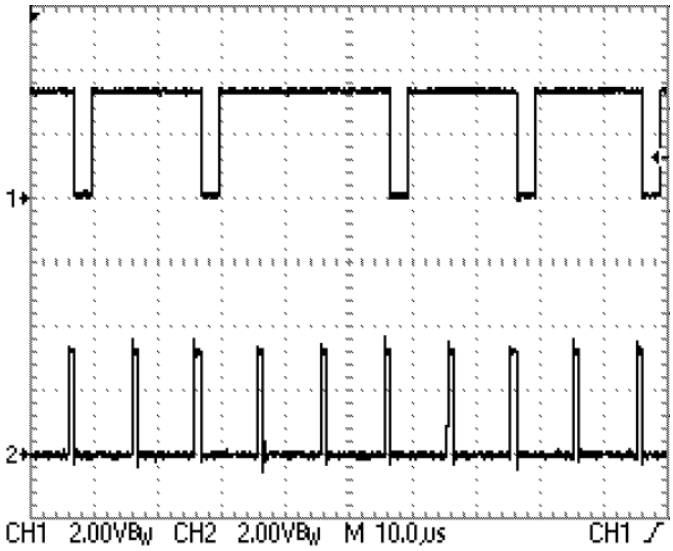

Fig. 11 Chip-select or "counter" (Ch1) and input signal to FPGA board (Ch2).

More tests were run to find out what could cause the timer to overflow. Code modifications of program "measure" were necessary and it fixed problem of unpredicted over-counting sometimes. All the data was sent within 3µs.

C. DC/DC power supply

As the signal of a transistor overlaps or dead-time is too small, current pikes are noticed at the input of the transformer's primary side windings (Fig. 12). This DC/DC converter later will be adapted to specific input voltage.

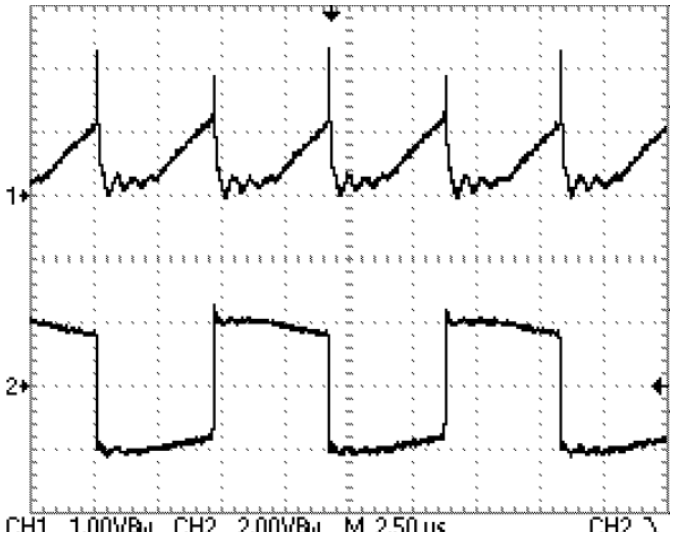

Fig. 12 The current (1) and the voltage (2) at the primary side of the transformer

D. *Power circuit test*

Power circuit tests were done and tested dead time between both transistors is approximately 1.6μs. For the load test purposes of power circuit, one leg were used from previous made full-bridge board. In this case control signal was taken from full-bridge board and the load type was inductive. The example is depicted by Fig. 13.

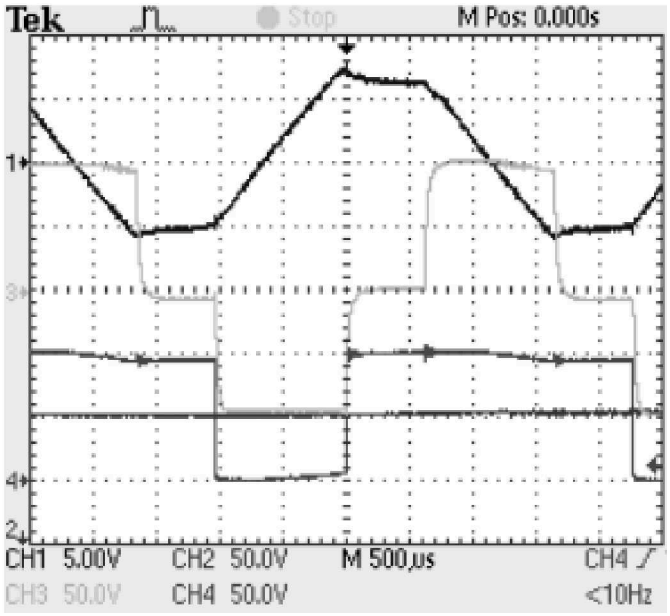

Fig. 13 Load test of power circuit: load current (1); DC voltage (2); AC output voltage (3) and drain to source voltage of one transistor (4).

VII. CONCLUSIONS

Programming of the FGPA board was done during the experimental research.

Characteristics of the influence of temperature on semiconductors can be taken from datasheets, but also can be tested and prescribed in the control program.

Developed measurement circuit can be used for measuring the voltage and as a frequency generator for a high frequency DC/DC power supply.

For future work, DC/DC power supply circuit should be improved by adding the voltage stabilization circuit at output and EMI tests should be done.

ACKNOWLEDGMENT

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REFERENCES

[1] K. Corzine "Operations and Design of Multilevel Inverters", Missouri, USA, 2003.
[2] A. Lesnicar and R. Marquardt "An innovative Modular Multilevel Converter Topology Suitable for a Wide Power Range", IEEI Bologna Power-Tech Conference, Bologna, Italy, 2003.
[3] M. Glinka and R. Marquardt "A New AC/AC Multilevel Converter Family", IEEI Transactions on industrial electronics, vol.52, June 2005.
[4] M. Hagiwara and H.Akagi "PWM Control and Experiment of Modular Multilevel Converters", Tokyo Institute of Technology, Japan.
[5] S. Allebrod, R. Hamerski, and R. Marquardt "New Transformerless, Scalable Modular Multilevel Converters for HVDC-Transmision", Institute of Power Electronics and Control, Germany.
[6] M. Glinka "Prototype of Mutiphase Modular-Multilevel-Converter with 2MW power rating and 17-level-voltage", Institute of Power Electronics and Control, Germany.
[7] R. Marquardt and A. Lesnicar "New Concept of High Voltage – Modular Multilevel Converter", PESC 2004 Conference, Aachen, Germany.
[8] A. Lesnicar and R. Marquardt "A New modular voltage source inverter topology", Institute of Power Electronics and Control, Germany.
[9] F. Ohlsson "Programming of a real-time Simulator for SVC and TCSC", Master of Science Thesis, Stockholm, Sweden 2006.