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# A PLL Scheme for Synchronization with Grid Voltage Phasor in Active Power Filter Systems

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***Abstract.*** **Voltage source inverters connected to the grid in applications such as active power filters require synchronization with the grid voltage. Since in practice the grid voltage can be unbalanced and distorted, but the operation of the whole active filter control system is strongly dependant on precise estimation of grid voltage phase, the fundamental positive sequence phasor of the grid voltage has to be extracted. In this paper a system for smooth estimation of the position of the voltage phasor at the point of common coupling of a parallel active filter system is presented using a sinusoidal signal integrator and a simple software PLL. The performance of the proposed system is verified by simulation and experimental results. The proposed PLL scheme can also be used in other vector oriented control systems.**

***Keywords:*** **active filters, phase locked loops**

## I. INTRODUCTION

Active power filters are a developing technology and several filter topologies have been proposed ever since the basic harmonic compensation principle was introduced in early seventies of the 20th century [1]. The parallel active power filter is connected in parallel with the nonlinear load and, in fact, is a current controlled voltage source PWM converter (Fig.1.). The main task of the control system of the parallel active filter is the control of the filter current in order to generate the compensating current which when summed with the current of the nonlinear load would create a sinusoidal supply current. The performance of the active filter as a controlled current source depends on the operation speed and accuracy of the current regulator implemented in the control system.

In many applications of current controlled voltage source converters (e.g., vector-controlled ac motor drives), where an ideally impressed current is required and the applied control scheme is based on the space-vector approach, even small phase errors can cause an incorrect operation of the system [2]. In the same way extraction of a correct current reference as well as the operation of the whole control system of the active power filter is strongly dependant on a precise estimation of the phase of the fundamental positive sequence phasor of the grid voltage at the point of common coupling (PCC). The harmonic distortion, if present in the grid voltage, affects the whole current control loop, because the synchronization phase signal used for the reference frame transformations is distorted.

A common technique used for determining the phase of a sinusoidal signal (or a phasor) is the so called phase-locked-loop (PLL). Generally, a PLL is a circuit synchronizing it output signal with a reference or input signal in frequency as well as in phase. In the synchronized state, the phase error between the system output signal and the reference signal is zero, or it remains constant [3].

In this paper a system for a smooth estimation of the position of the voltage phasor at the PCC of a parallel active filter system is presented using a sinusoidal signal integrator and a simple software PLL. The performance of the proposed system is verified by simulation and experimental results.

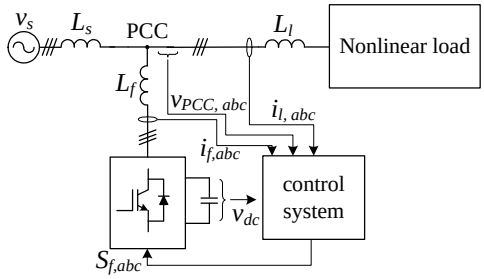


Fig.1. Parallel active power filter system.

## II. THE STRUCTURE OF THE PROPOSED PLL SYSTEM

The whole parallel active filter control system including the proposed PLL scheme is shown in Fig.2. As can be observed, before feeding the measured voltage to the PLL system, the three phase signal is transferred to stationary orthogonal αβ reference frame by the following equation:

$$\begin{pmatrix} v_\alpha \\ v_\beta \end{pmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \cdot \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \quad (1)$$

Since in practical applications the grid voltage can be distorted, but the operation of the whole control system of the active power filter is strongly dependant on a precise phase estimation of the fundamental positive sequence voltage phasor at the PCC, the voltage measurement has to be filtered – if the grid voltage distortion propagated in the phase signal, the reference frame transformations implemented in the current control loop would no longer be valid.

To overcome this problem a sinusoidal signal integrator (SSI) based voltage filter for unbalanced and/or distorted PCC voltage is presented in [4]. If a distorted, but balanced PCC

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voltage is considered, the proposed filter can be slightly simplified.

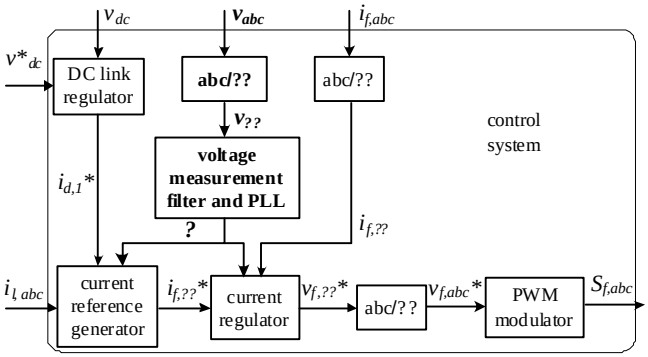


Fig.2. The location of the proposed PLL scheme in the parallel active filter control system.

SSI assures a zero steady state error for a sinusoidal input signal at its resonance frequency. SSI in fact is a resonance filter of the second order which in continuous time domain can be described by the following transfer function [6]:

$$H(s) = \frac{k_i \cdot s}{s^2 + \omega_0^2} \tag{2}$$

The discrete state-space model of the transfer function given in (2) is:

$$\begin{cases} \mathbf{x}_{k+1} = \mathbf{A}_d \cdot \mathbf{x}_k + \mathbf{B}_d \cdot u_k \\ y_k = x_{1k} \end{cases}, \tag{3}$$

where $\mathbf{x}_k = \begin{bmatrix} x_{1k} \\ x_{2k} \end{bmatrix}$ is the vector of states, $\mathbf{A}_d = \begin{bmatrix} \cos(\omega_0 T_s) & \sin(\omega_0 T_s) \\ -\sin(\omega_0 T_s) & \cos(\omega_0 T_s) \end{bmatrix}$, $\mathbf{B}_d = \frac{k_i}{\omega_0} \begin{bmatrix} \sin(\omega_0 T_s) \\ \cos(\omega_0 T_s) - 1 \end{bmatrix}$ and $T_s$ – the discrete time step.

Taking into account that states $x_1$ and $x_2$ of the SSI regulator in the stationary mode are sinusoidal and shifted by $90^0$C and assuming that the PCC voltage is balanced, it is possible to apply a SSI only for α component of the voltage vector, finding the β component from the state $x_2$ with its sign (which depends on the voltage phase sequence) determined at the initialization stage of the control algorithm. The proposed simplified version of SSI filter for PCC voltage measurement is shown on Fig.3.

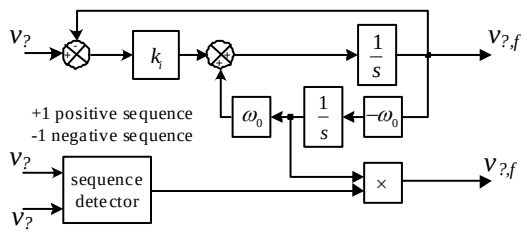


Fig.3. SSI filter for the PCC voltage measurement.

After extraction of the fundamental component of the PCC voltage in $\alpha\beta$ reference frame a simple PLL follows, containing a PI regulator in synchronous $dq$ reference frame applied to $v_q$ component (Fig.4.).

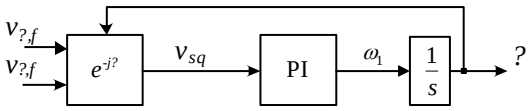


Fig.4. The PLL system with PI regulator in synchronous reference frame.

The voltage in the synchronous reference frame is obtained by the following coordinate transformation:

$$\mathbf{v}_{dq} = \mathbf{D}\mathbf{v}_{\alpha\beta}, \tag{4}$$

where $v_{dq}$ is the current vector in the synchronous reference frame, $v_{\alpha\beta}$ is the current vector in the stationary reference frame, D is a coordinate transformation matrix defined as:

$$\mathbf{D} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}, \tag{5}$$

but the position of the voltage phasor:

$$\theta = \arctan\frac{u_{t\alpha}}{u_{t\beta}}. \tag{6}$$

The PI regulator in stationary mode provides that the $v_q$ component of the voltage vector is zero, hence precisely aligning the synchronous reference frame with the instantaneous position of the phasor of the fundamental component of the PCC voltage (Fig.5.).

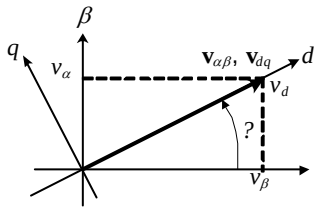


Fig.5. PCC voltage phasor in stationary and synchronous reference frames.

## III. SIMULATION OF THE PLL SYSTEM

The operation of the proposed PLL system was verified by simulation in Matlab/Simulink environment (Fig.6.). The model consists of a nonlinear load (a three-phase full bridge rectifier) connected to the grid voltage block, providing the injection of the $5^{th}$ and $7^{th}$ harmonic components into a balanced three phase voltage system in order to simulate the distorted mains conditions present at the site of the experimental testing. The proposed PLL scheme was realized as a C-code s-function located in the triggered subsystem. The whole model was constructed in close resemblance with the real life situation, where the PLL algorithm would be included in the control task of the active filter system and executed at the beginning of every switching period of the current controlled PWM inverter (which was not modeled here).

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The simulation results of a steady state system operation are shown on Fig.7. As can be seen at the top of the figure, there is a strong harmonic distortion (about 4%THD) present in the grid voltage – 7% 5th harmonic component, 5% 7th harmonic component as well as the harmonic distortion caused by the non-sinusoidal voltage drop in the source impedance due to the nonlinear load.

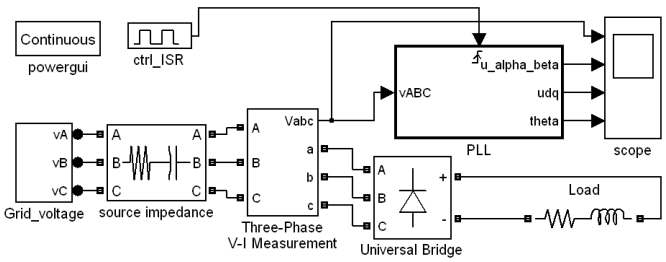


Fig.6. Matlab/Simulink model of the proposed PLL system.

As evident from the simulation results, the performance of the proposed PLL scheme is good – even at heavily distorted mains voltage, the estimation of the voltage phasor position is smooth.

## IV. Experimental results

The same s-function containing the PLL algorithm was used and compiled by the Matlab/Simulink RTI in order to load the code into the DSPACE control system prototyping platform and test experimentally. The Matlab/Simulink RTI implementation of the investigated system is shown on Fig.8a. The PLL algorithm together with the ADC task is executed in the interrupt service routine (ISR) subsystem of the main control task. The contents of the ISR subsystem are shown on Fig.8b. The grid line voltages (from a 25kVA power transformer) were connected to the ±10V ADC channels of the DSPACE platform through LV25-P voltage sensors.

The experimental data collected using Control Desk graphical user interface software of the DSPACE system are presented on Fig.9.

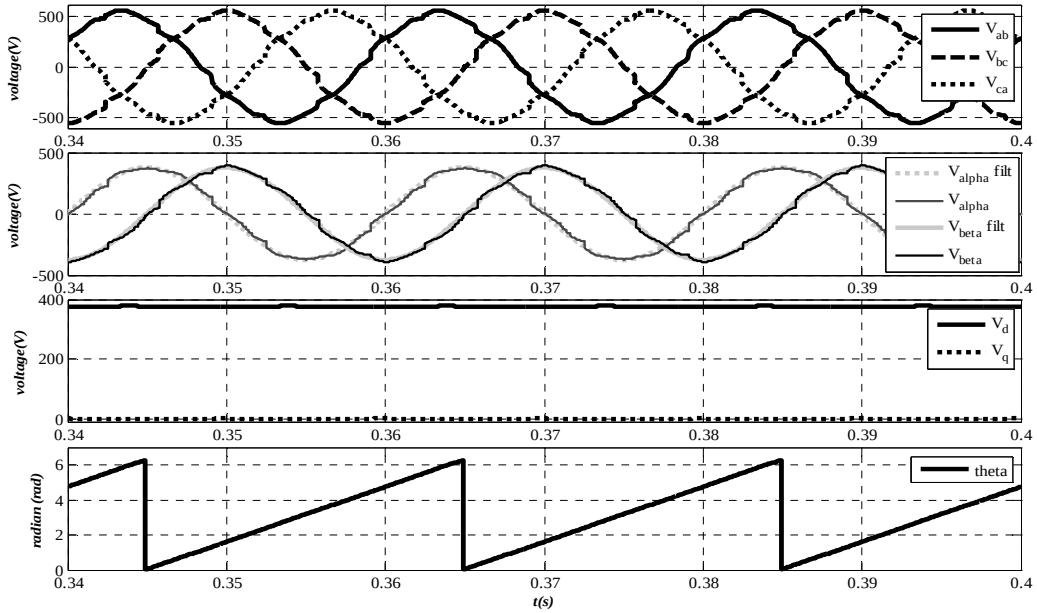


Fig.7. Simulated PLL characteristics with distorted voltage source – from top: PCC line voltages, voltage in the stationary αβ reference frame before and after the SSI filter, voltage in the synchronous dq reference frame and phase of the of the phasor of the fundamental component.

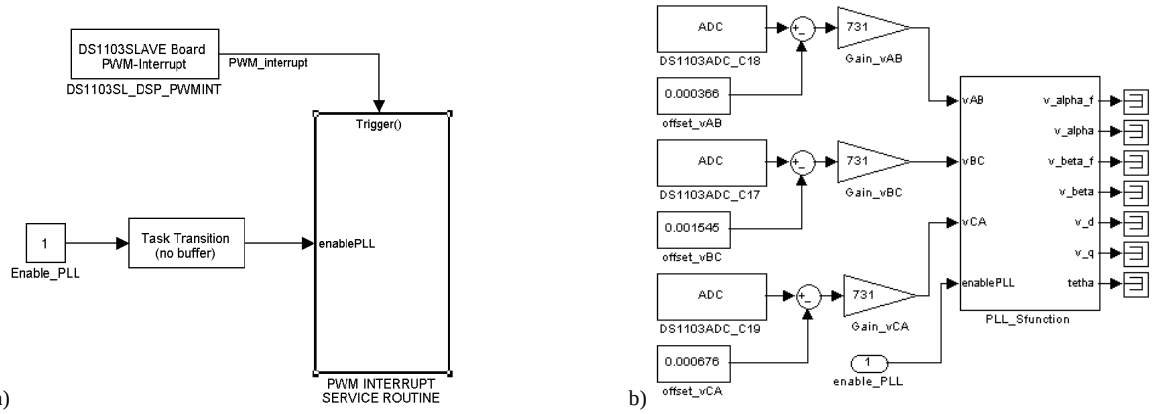


Fig.8. Matlab/Simulink implementation of the investigated system using DSPACE RTI tools: a) The main interrupt service routine block; b) PLL algorithm and the ADC task.

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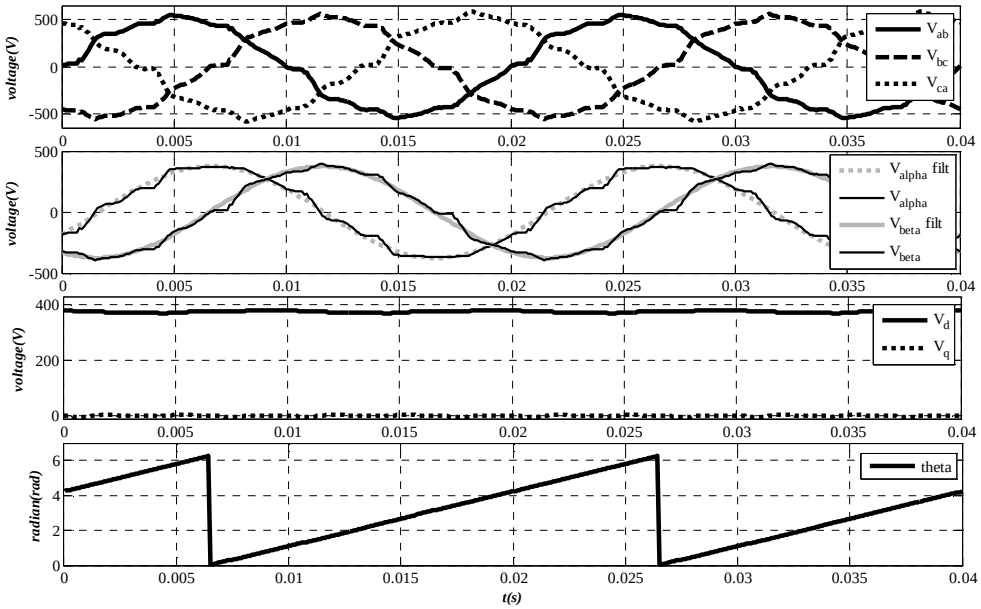


Fig.9. Experimentally acquired data – from top: PCC line voltages, voltage in the stationary αβ reference frame before and after the SSI filter, voltage in the synchronous dq reference frame and phase of the of the phasor of the fundamental component.

## V. CONCLUSIONS

A PLL scheme for precise estimation of the grid voltage phasor position in a parallel active filter system is elaborated. The PLL scheme is intended for balanced voltage conditions; hence a small error will be present in the estimated phasor position in case the grid voltage is considerably unbalanced.

The operation of the proposed PLL scheme has been verified by simulation and experimentally with practically coinciding results. The test results indicate a correct operation of the PLL scheme, providing a precise estimation of the position of fundamental positive sequence voltage phasor even though significant harmonic distortion is present in the grid voltage.

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